

SN74LVCC4245A

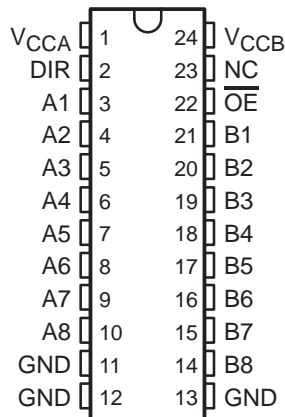
OCTAL DUAL-SUPPLY BUS TRANSCEIVER

WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

SCAS584L – NOVEMBER 1996 – REVISED AUGUST 2003

- Bidirectional Voltage Translator
- 4.5 V to 5.5 V on A Port and 2.7 V to 5.5 V on B Port
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DB, DW, NS, OR PW PACKAGE
(TOP VIEW)



NC – No internal connection

description/ordering information

This 8-bit (octal) noninverting bus transceiver uses two separate power-supply rails. The A port, V_{CCA} , is dedicated to accept a 5-V supply level, and the configurable B port, which is designed to track V_{CCB} , accepts voltages from 3 V to 5 V. This allows for translation from a 3.3-V to a 5-V environment and vice versa.

The SN74LVCC4245A is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (\overline{OE}) input can be used to disable the device so the buses are effectively isolated.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	SOIC – DW	Tube of 25	SN74LVCC4245ADW	LVCC4245A
		Reel of 2000	SN74LVCC4245ADWR	
	SOP – NS	Reel of 2000	SN74LVCC4245ANSR	LVCC4245A
	SSOP – DB	Reel of 2000	SN74LVCC4245ADBR	LG245A
	TSSOP – PW	Tube of 60	SN74LVCC4245APW	LG245A
		Reel of 2000	SN74LVCC4245APWR	
Reel of 250		SN74LVCC4245APWT		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE (each transceiver)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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recommended operating conditions (see Note 3)

			V _{CCA}	V _{CCB}	MIN	NOM	MAX	UNIT
V _{CCA}	Supply voltage				4.5	5	5.5	V
V _{CCB}	Supply voltage				2.7	3.3	5.5	V
V _{IHA}	High-level input voltage	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	4.5 V	2.7 V	2		V	
				3.6 V	2			
			5.5 V	5.5 V	2			
V _{IHB}	High-level input voltage	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	4.5 V	2.7 V	2		V	
				3.6 V	2			
			5.5 V	5.5 V	3.85			
V _{ILA}	Low-level input voltage	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	4.5 V	2.7 V	0.8		V	
				3.6 V	0.8			
			5.5 V	5.5 V	0.8			
V _{ILB}	Low-level input voltage	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	4.5 V	2.7 V	0.8		V	
				3.6 V	0.8			
			5.5 V	5.5 V	1.65			
V _{IH}	High-level input voltage (control pins)	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	4.5 V	3.6 V	2		V	
			5.5 V	5.5 V	2			
	High-level input voltage (control pins)	V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	4.5 V	2.7 V	2			
				3.6 V	2			
			5.5 V	5.5 V	2			
	V _{IL}	Low-level input voltage (control pins)	V _{OB} ≤ 0.1 V or V _{OB} ≥ V _{CCB} – 0.1 V	4.5 V	2.7 V	0.8		V
				3.6 V	0.8			
		5.5 V	5.5 V	0.8				
Low-level input voltage (control pins)		V _{OA} ≤ 0.1 V or V _{OA} ≥ V _{CCA} – 0.1 V	4.5 V	2.7 V	0.8			
				3.6 V	0.8			
			5.5 V	5.5 V	0.8			
V _{IA}	Input voltage			0	V _{CCA}		V	
V _{IB}	Input voltage			0	V _{CCB}		V	
V _{OA}	Output voltage			0	V _{CCA}		V	
V _{OB}	Output voltage			0	V _{CCB}		V	
I _{OHA}	High-level output current		4.5 V	3 V	–24		mA	
I _{OHB}	High-level output current		4.5 V	2.7 V to 4.5 V	–24		mA	
I _{OLA}	Low-level output current		4.5 V	3 V	24		mA	
I _{OLB}	Low-level output current		4.5 V	2.7 V to 4.5 V	24		mA	
T _A	Operating free-air temperature				–40	85		°C

NOTE 3: All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CCA}	V _{CCB}	MIN	TYP	MAX	UNIT
V _{OHA}		I _{OH} = -100 μA	4.5 V	3 V	4.4	4.49		V
		I _{OH} = -24 mA	4.5 V	3 V	3.76	4.25		
V _{OHB}		I _{OH} = -100 μA	4.5 V	3 V	2.9	2.99		V
		I _{OH} = -12 mA	4.5 V	2.7 V	2.2	2.5		
				3 V	2.46	2.85		
		I _{OH} = -24 mA	4.5 V	2.7 V	2.1	2.3		
				3 V	2.25	2.65		
4.5 V	3.76	4.25						
V _{OLA}		I _{OL} = 100 μA	4.5 V	3 V			0.1	V
		I _{OL} = 24 mA	4.5 V	3 V		0.21	0.44	
V _{OLB}		I _{OL} = 100 μA	4.5 V	3 V			0.1	V
		I _{OL} = 12 mA	4.5 V	2.7 V		0.11	0.44	
				3 V		0.21	0.44	
		I _{OL} = 24 mA	4.5 V	2.7 V		0.22	0.5	
3 V				0.21	0.44			
I _I	Control inputs	V _I = V _{CCA} or GND	5.5 V	3.6 V		±0.1	±1	μA
				5.5 V		±0.1	±1	
I _{OZ} [†]	A or B ports	V _O = V _{CCA/B} or GND, V _I = V _{IL} or V _{IH}	5.5 V	3.6 V		±0.5	±5	μA
I _{CCA}	B to A	A _n = V _{CC} or GND	5.5 V	Open		8	80	μA
		I _O (A port) = 0, B _n = V _{CCB} or GND	5.5 V	3.6 V		8	80	
I _{CCB}	A to B	A _n = V _{CCA} or GND, I _O (B port) = 0	5.5 V	3.6 V		5	50	μA
				5.5 V		8	80	
ΔI _{CCA} [‡]	A port	V _I = V _{CCA} - 2.1 V, Other inputs at V _{CCA} or GND, OE at GND and DIR at V _{CCA}	5.5 V	5.5 V		1.35	1.5	mA
	$\overline{\text{OE}}$	V _I = V _{CCA} - 2.1 V, Other inputs at V _{CCA} or GND, DIR at V _{CCA} or GND	5.5 V	5.5 V		1	1.5	
	DIR	V _I = V _{CCA} - 2.1 V, Other inputs at V _{CCA} or GND, OE at V _{CCA} or GND	5.5 V	3.6 V		1	1.5	
ΔI _{CCB} [‡]	B port	V _I = V _{CCB} - 0.6 V, Other inputs at V _{CCB} or GND, OE at GND and DIR at GND	5.5 V	3.6 V		0.35	0.5	mA
C _i	Control inputs	V _I = V _{CCA} or GND	Open	Open		5		pF
C _{io}	A or B ports	V _O = V _{CCA/B} or GND	5 V	3.3 V		11		pF

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

[‡] This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.



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switching characteristics over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see Figures 1 through 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$, $V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		$V_{CCA} = 5\text{ V} \pm 0.5\text{ V}$, $V_{CCB} = 2.7\text{ V TO } 3.6\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
t_{PHL}	A	B	1	7.1	1	7	ns
t_{PLH}			1	6	1	7	
t_{PHL}	B	A	1	6.8	1	6.2	ns
t_{PLH}			1	6.1	1	5.3	
t_{PZL}	\overline{OE}	A	1	9	1	9	ns
t_{PZH}			1	8.3	1	8	
t_{PZL}	\overline{OE}	B	1	8.2	1	10	ns
t_{PZH}			1	8.1	1	10.2	
t_{PLZ}	\overline{OE}	A	1	4.7	1	5.2	ns
t_{PHZ}			1	4.9	1	5.2	
t_{PLZ}	\overline{OE}	B	1	5.4	1	5.4	ns
t_{PHZ}			1	6.3	1	7.4	

operating characteristics, $V_{CCA} = 5\text{ V}$, $V_{CCB} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	$C_L = 0$, $f = 10\text{ MHz}$	20	pF
			6.5	

power-up considerations†

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device pins. Take these precautions to guard against such power-up problems.

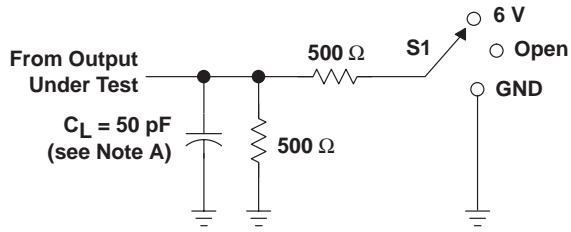
1. Connect ground before any supply voltage is applied.
2. Next, power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie \overline{OE} to V_{CCA} with a pullup resistor so that it ramps with V_{CCA} .
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA} . Otherwise, keep DIR low.

† Refer to the TI application report, *Texas Instruments Voltage-Level-Translation Devices*, literature number SCEA021.

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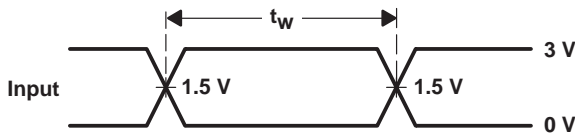
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PARAMETER MEASUREMENT INFORMATION FOR A TO B
 $V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$ AND $V_{CCB} = 2.7\text{ V TO }3.6\text{ V}$

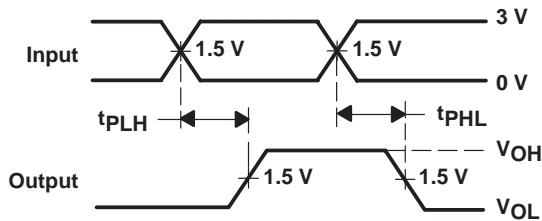


LOAD CIRCUIT

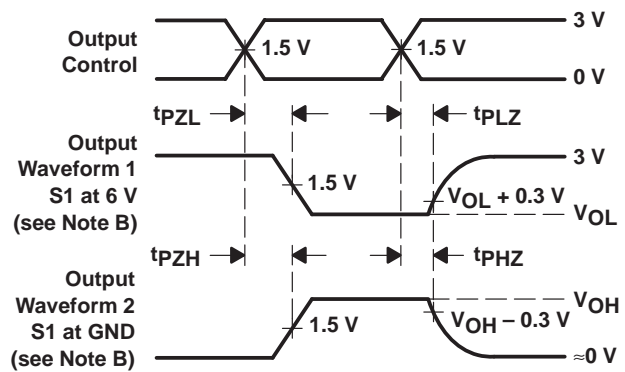
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

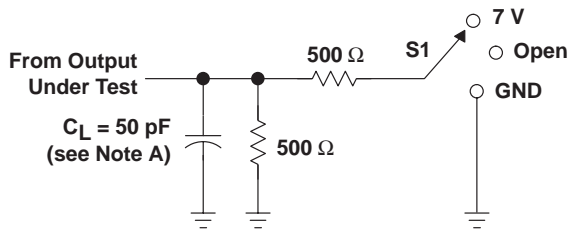
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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WITH CONFIGURABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

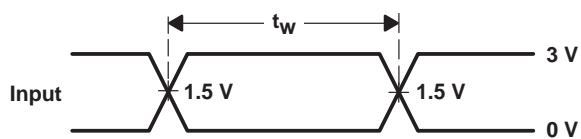
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PARAMETER MEASUREMENT INFORMATION FOR A TO B
 $V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$ AND $V_{CCB} = 3.6\text{ V TO }5.5\text{ V}$

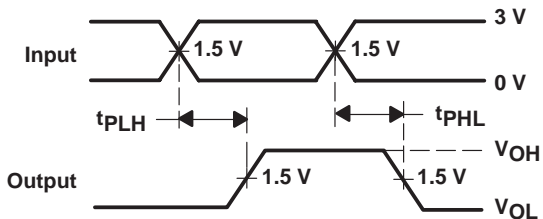


LOAD CIRCUIT

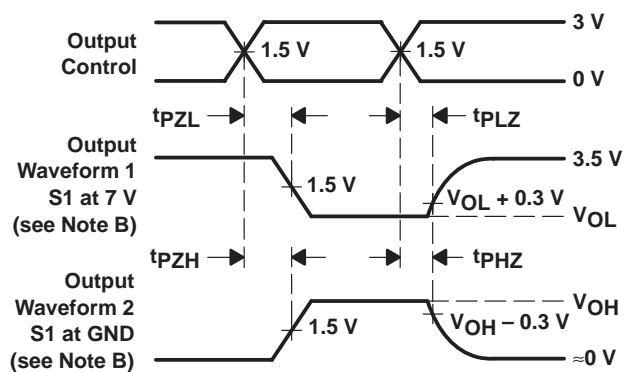
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

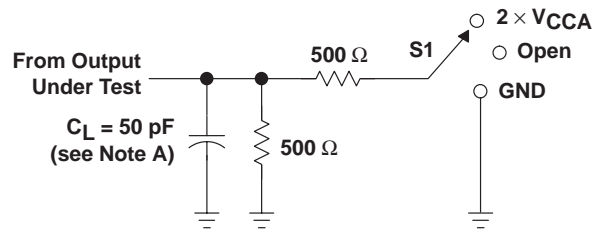
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

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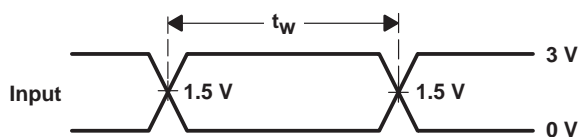
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PARAMETER MEASUREMENT INFORMATION FOR B TO A
 $V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$ AND $V_{CCB} = 2.7\text{ V TO }3.6\text{ V}$

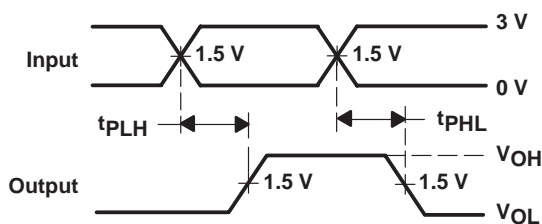


LOAD CIRCUIT

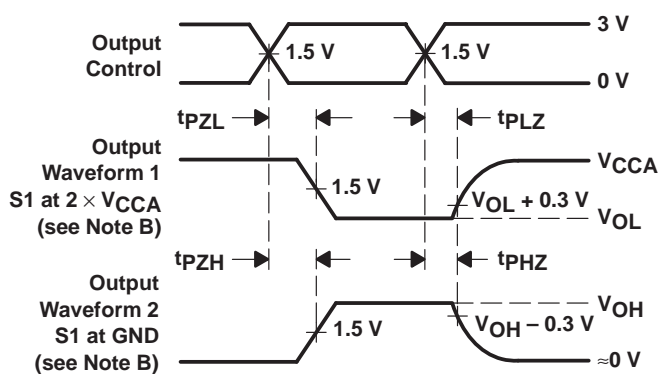
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCA}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

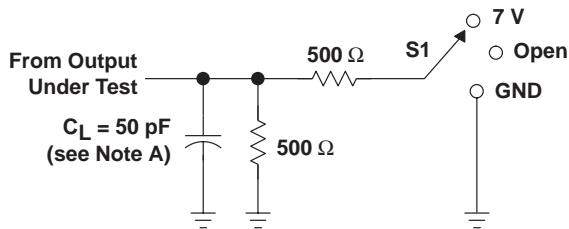
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

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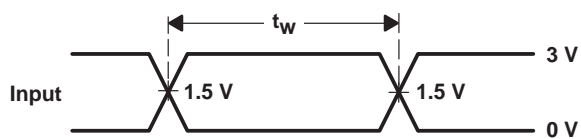
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PARAMETER MEASUREMENT INFORMATION FOR B TO A
 $V_{CCA} = 4.5\text{ V TO }5.5\text{ V}$ AND $V_{CCB} = 3.6\text{ V TO }5.5\text{ V}$

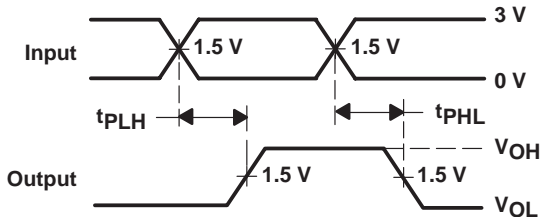


LOAD CIRCUIT

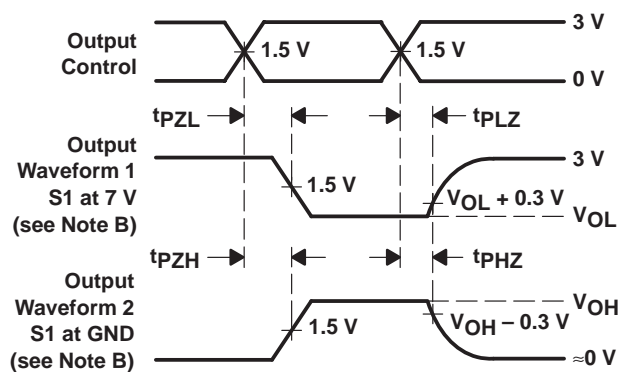
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND



**VOLTAGE WAVEFORMS
PULSE DURATION**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING**

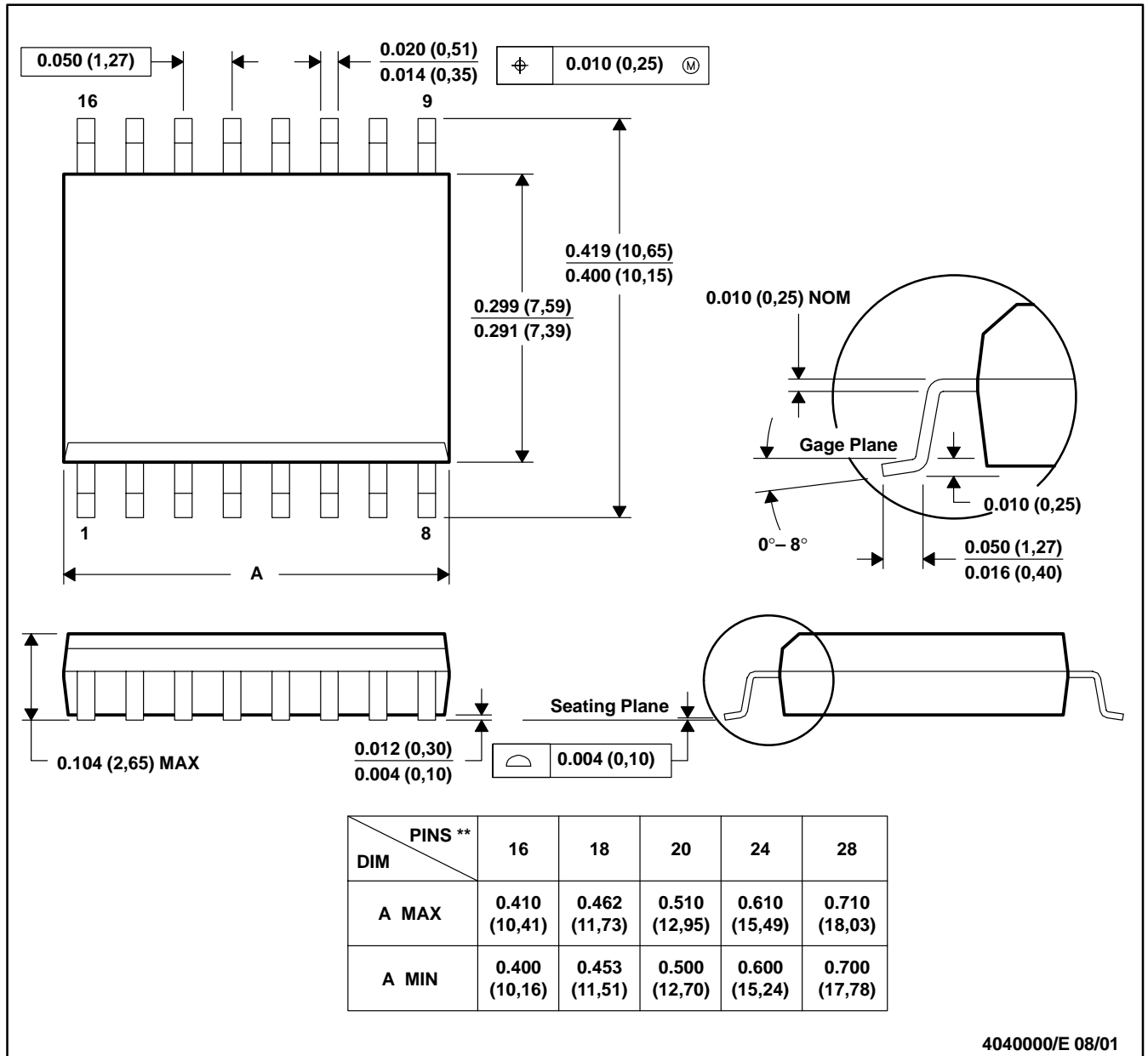
- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 2.5\text{ ns}$, $t_f \leq 2.5\text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

DW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

16 PINS SHOWN



4040000/E 08/01

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-013

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

4040065 /E 12/01

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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