

CHANGED

14M /CLRGT RESTRG /RST A6 A7 /SELIO /ROMEN1 /ROMEN2 GND /OE /RSTC /ROMEN /RSTB
/RSTA CREF 7M /DEV56 BURST UCC

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IF (CLRGT) BURST = CREF
IF (UCC) DEV56 = A6 * A7 * SELIO
IF (UCC) ROMEN = ROMEN1 + ROMEN2
7M := 7M
CREF := 7M * CREF + /7M * /CREF
RSTA := /RSTA * /RSTB * RST * /RESTRG +
        /RSTA * RSTB * /RESTRG +
        /RSTB * RSTA +
        RSTA * RSTB * RESTRG
RSTB := RESTRG * RSTA +
        /RSTA * /RSTB * RST * RESTRG +
        RESTRG * /RSTA * RSTB
IF (UCC) RSTC = RSTA + RSTB

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DESCRIPTION No comment at this time!
=

PASS
+XPLOTT

#P

00	-X-	----	----	----	----	----	----
01	----	----	----	--X-	----	----	----
08	----	----	----	----	----	----	----
09	----	----	----	X--	X--	X--	----
16	----	----	--X-	----	----	----	----
24	----	----	--X-	--X-	----	----	----
25	----	----	---X	---X	----	----	----
32	----	-X-	-X-	----	--X-	--X-	----
33	----	-X-	----	----	--X-	--X-	----
34	----	----	----	----	---X	---X	----
35	----	X--	----	----	---X	---X	----
40	----	X--	----	----	---X	----	----
41	----	X--	-X-	----	--X-	--X-	----
42	----	X--	----	----	--X-	--X-	----
48	----	----	----	----	----	----	----
49	----	----	----	----	----	----	-X-
50	----	----	----	----	----	----	-X-
56	----	----	----	----	----	----	----
57	----	----	----	----	---	X	----
58	----	----	----	----	---	X	----

OUTPUT

PAL16P8 B. COLVIN & W. BROEDNER
 REV ET-1 10/01/82
 APPLE][et TIMING STATE MACHINE

14M 7M CREF H0 UID07 SE6B GR /RAMEN /800COL GND /OE LOPS UID7M PHASE1 PHASE0 Q3 C
 AS AX RAS UCC

UID7M:= /GR*7M+
 PHASE0*UID7M*/SE6B*GR+
 GR*/SE6B*Q3*UID7M+
 AX*/SE6B*GR*UID7M+
 /PHASE0*/AX*/Q3*GR*/SE6B*/UID07+
 /PHASE0*/AX*/Q3*GR*/SE6B*/H0*CREF+
 GR*SE6B+
 /GR*800COL

10-14-82
B.C.

LOPS:= /PHASE0*/RAS*/Q3*7M*GR*/SE6B*/UID07+
 /PHASE0*/RAS*/Q3*/7M*GR*/SE6B*UID07+
 /PHASE0*/AX*/Q3*GR*SE6B+
 /PHASE0*/AX*/Q3*/GR+
 PHASE0*/AX*/Q3*/GR*800COL+
 /PHASE0*/AX*/Q3*GR*/SE6B*/H0*CREF

PHASE0:= PHASE0*RAS*/Q3+
 /PHASE0*Q3+
 /PHASE0*/RAS

PHASE1:= /PHASE0*RAS*/Q3+
 PHASE0*Q3+
 PHASE0*/RAS

RAS:= Q3+
 /PHASE0*/RAS*7M+
 PHASE0*/AX*/7M+
 PHASE0*AX*7M*H0*CREF+
 PHASE0*AX*/7M*H0*/CREF

AX:= /RAS*Q3

CAS:= /PHASE0*/RAS*/AX*CAS+
 PHASE0*/RAS*/AX*CAS*RAMEN+
 /RAS*/CAS

Q3:= /PHASE0*/AX*/7M+
 /RAS*/Q3+
 PHASE0*/AX*7M

DESCRIPTION: THIS STATE MACHINE GENERATES CONTROL AND TIMING
 SIGNALS FOR THE CPU, RAM, I/O CONNECTORS, AND
 VIDEO CIRCUITRY.

PASS
+X PLOT

#P

00	----	----	----	-X-	----	----	----	----		
01	X--X	----	----	----	---	X	----	----		
02	-X--	---X	----	----	----	-X-	----	----		
03	X--	X-X	X--	----	----	-X-	----	----		
04	-X--	-XX-	X--	----	----	-X-	----	----		
08	---	X	----	----	-X-	----	----	----		
16	---	X	---	X	----	---	X	----		
17	---	X	---	X	----	---	X	----		
18	---	X	---	X	----	----	----	----		
24	-X--	---	X	----	----	---	X	----		
25	---	X	----	----	---	X	----	----		
26	X--	---	X	----	----	---	X	----		
32	--X-	----	----	---	X	---	X	----		
33	----	----	----	---	X	---	X	----		
34	---	X	----	----	---	X	----	----		
40	--X-	----	----	---	X	---	X	----		
41	----	----	----	---	X	---	X	----		
42	---	X	----	----	---	X	----	----		
48	X--	----	----	----	----	---	X	----		
49	----	----	----	----	---	XX	X	---	X	
50	----	----	----	---	X	---	X	---	X	
51	----	---	X	----	---	X	---	X	---	X
52	----	---	X	----	---	X	---	X	---	X
53	----	X	---	X	---	X	---	X	---	X
54	----	----	----	----	---	X	---	X	----	----
55	----	----	----	----	----	---	X	----	---	X
6	X--X	----	----	---	X	---	X	---	X	----
57	-X-X	----	----	---	X	---	X	---	X	----
58	----	---	X	----	---	X	---	X	----	----
59	----	---	X	----	---	X	---	X	----	----
60	----	---	X	----	---	X	---	X	----	----
61	----	X	---	X	---	X	---	X	----	----

10-14-82
B.C.