Programmable Sound Generator

FEATURES
- Full Software Control of Sound Generation
- Interfaces to Most 8-Bit and 16-Bit Microprocessors
- Three Independently Programmed Analog Outputs
- Two 8-Bit General Purpose I/O Ports (AY-3-8910)
- One 8-Bit General Purpose I/O Port (AY-3-8912)
- Single +5 Volt Supply

DESCRIPTION
The AY-3-8910/8912/8913 Programmable Sound Generator (PSG) is a LSI Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912/8913 is manufactured in the General Instrument N-Channel Ion Implant Process. Operation requires a single +5V power supply, a TTL compatible clock, and a microprocessor controller such as the General Instrument 16-bit CP1610 or one of the PIC1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion, greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads; the AY-3-8913 has no ports and 24 leads.

PIN FUNCTIONS
DA7--DA0 (input/output/high impedance): pins 30--37 (AY-3-8910)
Data/Address 7--0: pins 21--28 (AY-3-8912)
pins 4--11 (AY-3-8913)

These 8 lines comprise the 8-bit bidirectional bus used by the microprocessor to send both data and addresses to the PSG and to receive data from the PSG. In the data mode, DA7--DA0 correspond to Register Array bits B7--B0. In the address mode, DA3--DA0 select the register number ($0\text{--}17_8$) and a DA7--DA4 in conjunction with address inputs $\overline{A9}$ and A8 for the high order address (chip select).

A8 (input): pin 25 (AY-3-8910)
pin 17 (AY-3-8912)
pin 23 (AY-3-8913)

$\overline{A9}$ (input): pin 24 (AY-3-8910)
pin 22 (AY-3-8913)
(not provided on AY-3-8912)

Address 9, Address 8

These "extra" address bits are made available to enable the positioning of the PSG (assigning a 16 word memory space) in a total 1,024 word memory area rather than in a 256 word memory area as defined by address bits DA7--DA0 alone. If the memory size does not require the use of these extra address lines they may be left unconnected as each is provided with either an on-chip pull down ($\overline{A9}$) or pull-up (A8) resistor. In "noisy" environments, however, it is recommended that $\overline{A9}$ and A8 be tied to an external ground and +5V, respectively, if they are not to be used.

PIN CONFIGURATIONS

40 LEAD DUAL IN LINE
AY-3-8910

Top View

V_{SS} (GND)	1	40	V_{CC} (+5V)
N.C.	2	39	TEST 1
ANALOG CHANNEL B	3	38	ANALOG CHANNEL C
ANALOG CHANNEL A	4	37	DA0
N.C.	5	36	DA1
IOB7	6	35	DA2
IOB6	7	34	DA3
IOB5	8	33	DA4
IOB4	9	32	DA5
IOB3	10	31	DA6
IOB2	11	30	DA7
IOB1	12	29	BC1
IOB0	13	28	BC2
IOA7	14	27	BDIR
IOA6	15	26	TEST 2
IOA5	16	25	A8
IOA4	17	24	$\overline{A9}$
IOA3	18	23	$\overline{RESET}$
IOA2	19	22	CLOCK
IOA1	20	21	IOA0

28 LEAD DUAL IN LINE
AY-3-8912

Top View

ANALOG CHANNEL C	1	28	DA0
TEST 1	2	27	DA1
V_{CC} (+5V)	3	26	DA2
ANALOG CHANNEL B	4	25	DA3
ANALOG CHANNEL A	5	24	DA4
V_{SS} (GND)	6	23	DA5
IOA7	7	22	DA6
IOA6	8	21	DA7
IOA5	9	20	BC1
IOA4	10	19	BC2
IOA3	11	18	BDIR
IOA2	12	17	A8
IOA1	13	16	$\overline{RESET}$
IOA0	14	15	CLOCK

24 LEAD DUAL IN LINE

Top View

V_{SS} (GND)	1	24	$\overline{CHIP\ SELECT}$
BDIR	2	23	A8
BC1	3	22	$\overline{A9}$
DA7	4	21	$\overline{RESET}$
DA6	5	20	CLOCK
DA5	6	19	V_{SS} (GND)
DA4	7	18	ANALOG C
DA3	8	17	ANALOG A
DA2	9	16	NO CONNECT
DA1	10	15	ANALOG B
DA0	11	14	TEST IN
TEST OUT	12	13	V_{CC}

AUDIO

RESET (input): pin 23 (AY-3-8910) pin 21 (AY-3-8913)
pin 16 (AY-3-8912)

For initialization/power-on purposes, applying a logic "0" (ground) to the Reset pin will reset all registers to "0". The Reset pin is provided with an on-chip pull-up resistor.

CLOCK (input): pin 22 (AY-3-8910) pin 20 (AY-3-8913)
pin 15 (AY-3-8912)

This TTL-compatible input supplies the timing reference for the Tone, Noise and Envelope Generators.

BDIR, BC2, BC1 (inputs): pins 27,28,29 (AY-3-8910)
pins 18,19,20 (AY-3-8912) pins 2, 3 (No BC2 on AY-3-8913 see below).

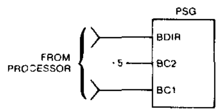
Bus DIRection, Bus Control 2,1

These bus control signals are generated directly by the CP1610 series of microprocessors to control all external and internal bus operations in the PSG. When using a processor other than the CP1610, these signals can be provided either by comparable bus signals or by simulating the signals on I/O lines of the processor. The PSG decodes these signals as illustrated in the following:

BDIR	BC2	BC1	CP1610 FUNCTION	PSG FUNCTION
0	0	0	NACT	INACTIVE. See 010 (IAB).
0	0	1	ADAR	LATCH ADDRESS. See 111 (INTAK).
0	1	0	IAB	INACTIVE. The PSG/CPU bus is inactive. DA7--DA0 are in a high impedance state.
0	1	1	DTB	READ FROM PSG. This signal causes the contents of the register which is currently addressed to appear on the PSG/CPU bus. DA7--DA0 are in the output mode.
1	0	0	BAR	LATCH ADDRESS. See 111 (INTAK).
1	0	1	DW	INACTIVE. See 010 (IAB).
1	1	0	DWS	WRITE TO PSG. This signal indicates that the bus contains register data which should be latched into the currently addressed register. DA7--DA0 are in the input mode.
1	1	1	INTAK	LATCH ADDRESS. This signal indicates that the bus contains a register address which should be latched in the PSG. DA7--DA0 are in the input mode.

While interfacing to a processor other than the CP1610 would simply require simulating the above decoding, the redundancies in the PSG functions vs. bus control signals can be used to advantage in that only four of the eight possible decoded bus functions are required by the PSG. This could simplify the programming of the bus control signals to the following, which would only require that the processor generate two bus control signals (BDIR and BC1, with BC2 tied to +5V). This is the case with the AY-3-8913 with BC2 pulled high internally.

BDIR	BC2	BC1	PSG FUNCTION
0	1	0	INACTIVE.
0	1	1	READ FROM PSG.
1	1	0	WRITE TO PSG.
1	1	1	LATCH ADDRESS.



ANALOG CHANNEL A, B, C (outputs): pins 4, 3, 38 (AY-3-8910)
pins 5, 4, 1 (AY-3-8912) pins 17, 15, 18 (AY-3-8913)

Each of these signals is the output of its corresponding D/A Converter, and provides an up to 1V peak-peak signal representing the complex sound waveshape generated by the PSG.

IOA7--IOA0 (input/output): pins 14--21 (AY-3-8910)
pins 7--14 (AY-3-8912) (not provided on AY-3-8913)

IOB7--IOB0 (input/output): pins 6--13 (AY-3-8910)
(not provided on AY-3-8912) (not provided on AY-3-8913)

Input/Output A7--A0, B7--B0

Each of these two parallel input/output ports provides 8 bits of parallel data to/from the PSG/CPU bus from/to any external devices connected to the IOA or IOB pins. Each pin is provided with an on-chip pull-up resistor, so that when in the "input" mode, all pins will read normally high. Therefore, the recommended method for scanning external switches would be to ground the input bit.

TEST 1: pin 39 (AY-3-8910) pin 14 (AY-3-8913) pin 2 (AY-3-8912)
TEST 2: pin 26 (AY-3-8910) pin 12 (AY-3-8913)
(not connected on AY-3-8912)

These pins are for General Instrument test purposes only and should be left open—do not use as tie-points.

V_{CC}: pin 40 (AY-3-8910) pin 13 (AY-3-8913) pin 3 (AY-3-8912)
Nominal +5Volt power supply to the PSG.

V_{SS}: pin 1 (AY-3-8910) pin 19 (AY-3-8913) pin 6 (AY-3-8912)
Ground reference for the PSG.

CHIP SELECT (Input) Pin 24 (AY-3-8913 only)

This input signal goes low to enable the PSG to read data on the data bus or write data from the data bus to one of the internal registers. For these above operations to occur, this signal must be true in addition to the current bus address being a valid PSG address. This signal must be valid for all read and write operations. The pin has an internal pull down to V_{SS}.

ARCHITECTURE

The AY-3-8910/8912/8913 is a register oriented Programmable Sound Generator (PSG). Communication between the processor and the PSG is based on the concept of memory-mapped I/O. Control commands are issued to the PSG by writing to 16 memory-mapped registers. Each of the 16 registers within the PSG is also readable so that the microprocessor can determine, as necessary, present states or stored data values.

All functions of the PSG are controlled through the 16 registers which once programmed, generate and sustain the sounds, thus freeing the system processor for other tasks.

REGISTER ARRAY

The principal element of the PSG is the array of 16 read/write control registers. These 16 registers look to the CPU as a block of memory and as such occupy a 16 word block out of 1,024 possible addresses. The 10 address bits (8 bits on the common data/address bus, and 2 separate address bits A8 and $\overline{A9}$) are decoded as follows:

$^*\overline{A9}$	A8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
0	1	0	0	0	0	0	0	0	0
THRU									
0	1	0	0	0	0	1	1	1	1
HIGH ORDER (Chip Select)						LOW ORDER (Register No.)			

* $\overline{A9}$ is not provided on the AY-3-8912.

The four low order address bits select one of the 16 registers (R0--R17$_8$). The six high order address bits function as "chip selects" to control the tri-state bidirectional buffers (when the high order address bits are "incorrect", the bidirectional buffers are forced to a high impedance state). High order address bits $\overline{A9}$, A8 are fixed in the PSG design to recognize a 01 code; high order address bits DA7--DA4 may be mask-programmed to any 4-bit code by a special order factory mask modification. Unless otherwise specified, address bits DA7--DA4 are programmed to recognize only a 0000 code. A valid high order address latches the register address (the low order 4 bits) in the Register Address Latch/Decoder block. A latched address will remain valid until the receipt of a new address, enabling multiple reads and writes of the same register contents without the need for redundant re-addressing.

Conditioning of the Register Address Latch/Decoder and the Bidirectional Buffers to recognize the bus function required (inactive, latch address, write data, or read data) is accomplished by the Bus Control Decode block.

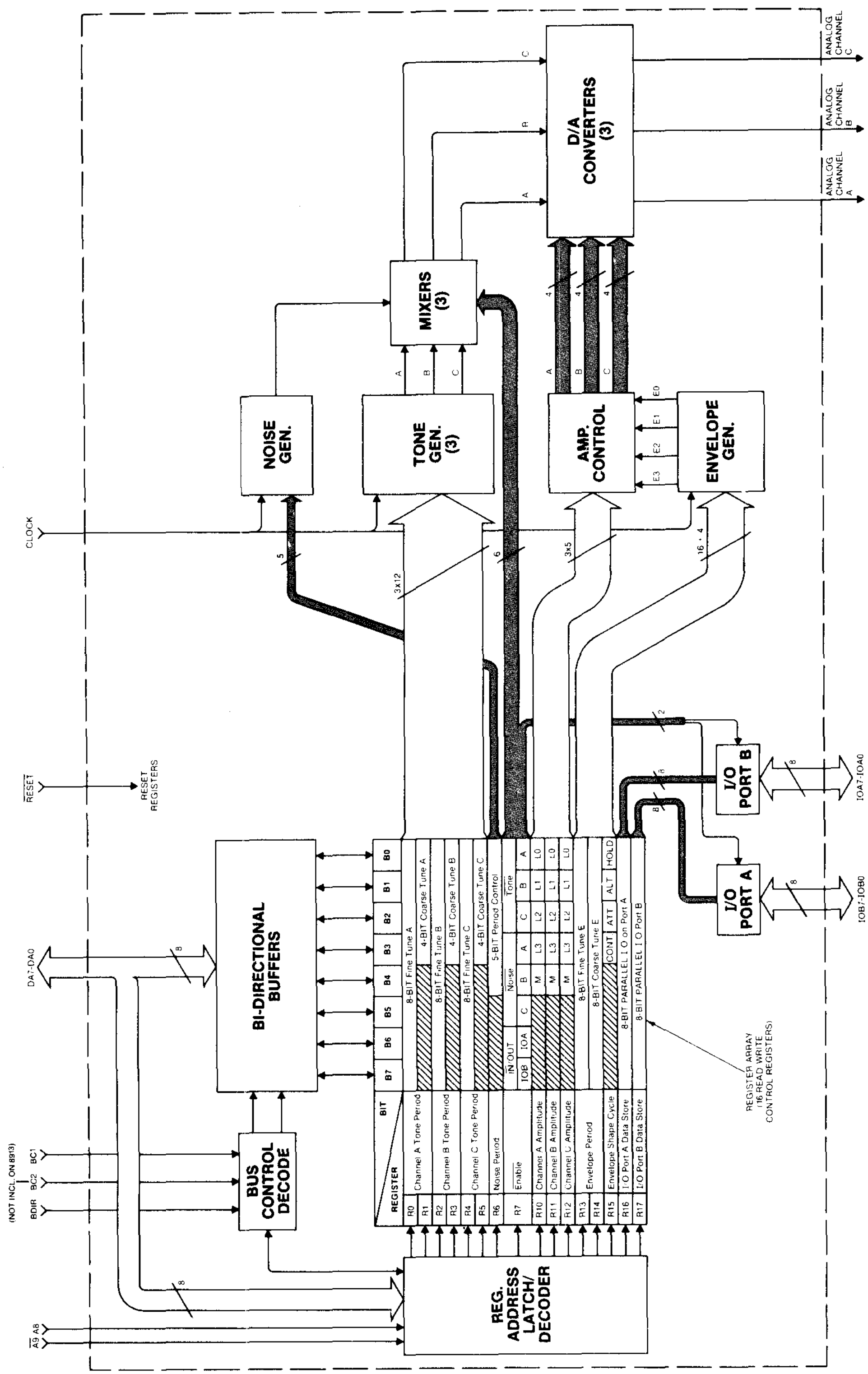
SOUND GENERATING BLOCKS

The basic blocks in the PSG which produce the programmed sounds include:

Tone Generators	produce the basic square wave tone frequencies for each channel (A,B,C)
Noise Generator	produces a frequency modulated pseudo random pulse width square wave output.
Mixers	combine the outputs of the Tone Generators and the Noise Generator. One for each channel (A,B,C).
Amplitude Control	provides the D/A Converters with either a fixed or variable amplitude pattern. The fixed amplitude is under direct CPU control; the variable amplitude is accomplished by using the output of the Envelope Generator.
Envelope Generator	produces an envelope pattern which can be used to amplitude modulate the output of each Mixer.
D/A Converters	the three D/A Converters each produce up to a 16 level output signal as determined by the Amplitude Control.

I/O PORTS

Two additional blocks are shown in the PSG Block Diagram which have nothing directly to do with the production of sound—these are the two I/O Ports (A and B). Since virtually all uses of microprocessor-based sound would require interfacing between the outside world and the processor, this facility has been included in the PSG. Data to/from the CPU bus may be read/written to either of two 8-bit I/O Ports without affecting any other function of the PSG. The I/O Ports are TTL-compatible and are provided with internal pull-ups on each pin. Both Ports are available on the AY-3-8910; only I/O Port A is available on the AY-3-8912; no ports are available on the AY-3-8913.



PSG BLOCK DIAGRAM

OPERATION

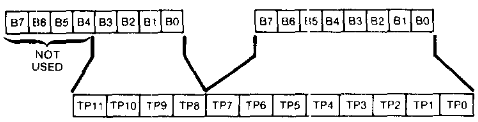
Since all functions of the PSG are controlled by the processor via a series of register loads, a detailed description of the PSG operation can best be accomplished by relating each PSG function to the control of its corresponding register. The function of creating or programming a specific sound or sound effect logically follows the control sequence listed:

Operation	Registers	Function
Tone Generator Control	R0--R5	Program tone periods.
Noise Generator Control	R6	Program noise period.
Mixer Control	R7	Enable tone and/or noise on selected channels.
Amplitude Control	R10--R12	Select "fixed" or "envelope-variable" amplitudes.
Envelope Generator Control	R13--R15	Program envelope period and select envelope pattern

Tone Generator Control
(Registers R0, R1, R2, R3, R4, R5)

The frequency of each square wave generated by the three Tone Generators (one each for Channels A, B, and C) is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 12-bit Tone Period value. Each 12-bit value is obtained in the PSG by combining the contents of the relative Coarse and Fine Tune registers, as illustrated in the following:

Coarse Tune Register	Channel	Fine Tune Register
R1	A	R0
R3	B	R2
R5	C	R4

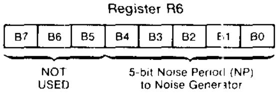


12-bit Tone Period (TP) to Tone Generator

Noise Generator Control
(Register R6)

The frequency of the noise source is obtained in the PSG by first counting down the input clock by 16, then by further counting down the result by the programmed 5-bit Noise Period value. This 5-bit value consists of the lower 5 bits (B4--B0) of register R6, as illustrated in the following:

Noise Period
Register R6



Mixer Control-I/O Enable
(Register R7)

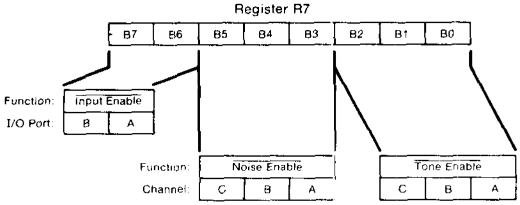
Register R7 is a multi-function Enable register which controls the three Noise/Tone Mixers and the two general purpose I/O Ports.

The Mixers, as previously described, combine the noise and tone frequencies for each of the three channels. The determination of combining neither/either/both noise and tone frequencies on each channel is made by the state of bits B5--B0 of R7.

The direction (input or output) of the two general purpose I/O Ports (IOA and IOB) is determined by the state of bits B7 and B6 of R7.

These functions are illustrated in the following:

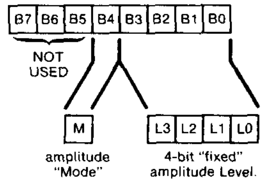
Mixer Control-I/O Enable
Register R7



Amplitude Control
(Registers R10, R11, R12)

The amplitudes of the signals generated by each of the three D/A Converters (one each for Channels A, B, and C) is determined by the contents of the lower 5 bits (B4--B0) of registers R10, R11, and R12 as illustrated in the following:

Amplitude Control Register	Channel
R10	A
R11	B
R12	C

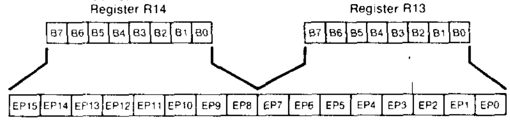


Envelope Generator Control
(Registers R13, R14, R15)

To accomplish the generation of fairly complex envelope patterns, two independent methods of control are provided in the PSG: first, it is possible to vary the frequency of the envelope using registers R13 and R14; and second, the relative shape and cycle pattern of the envelope can be varied using register R15. The following paragraphs explain the details of the envelope control functions, describing first the envelope period control and then the envelope shape/cycle control.

ENVELOPE PERIOD CONTROL (Registers R13, R14)

The frequency of the envelope is obtained in the PSG by first counting down the input clock by 256, then by further counting down the result by the programmed 16-bit Envelope Period value. This 16-bit value is obtained in the PSG by combining the contents of the Envelope Coarse and Fine Tune registers, as illustrated in the following:



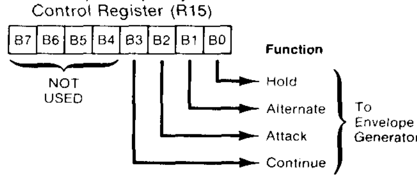
16-bit Envelope Period (EP) to Envelope Generator

ENVELOPE SHAPE/CYCLE CONTROL (Register R15)

The Envelope Generator further counts down the envelope frequency by 16, producing a 16-state per cycle envelope pattern as defined by its 4-bit counter output, E3 E2 E1 E0. The particular shape and cycle pattern of any desired envelope is accomplished by controlling the count pattern (count up/count down) of the 4-bit counter and by defining a single-cycle or repeat-cycle pattern.

This envelope shape/cycle control is contained in the lower 4 bits (B3--B0) of register R15. Each of these 4 bits controls a function in the envelope generator, as illustrated in the following:

Envelope Shape/Cycle
Control Register (R15)



AUDIO

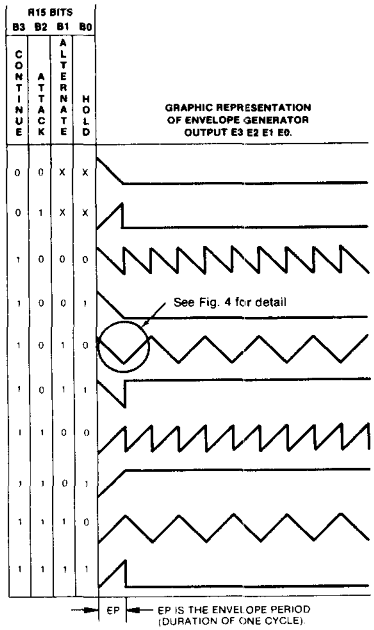


Fig. 1 ENVELOPE SHAPE/CYCLE OPERATION

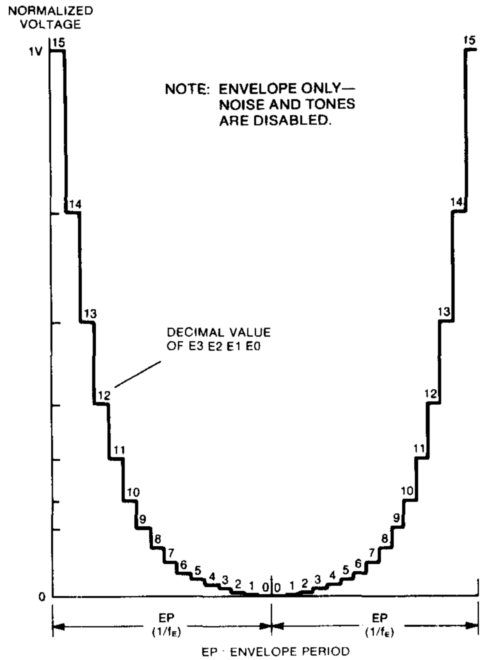


Fig. 3 D/A CONVERTER OUTPUT

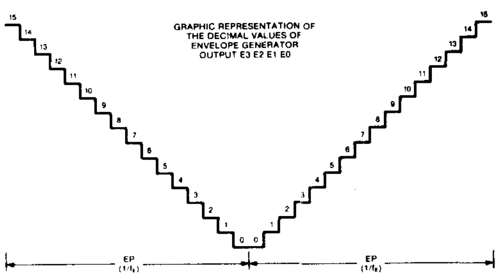


Fig. 2 DETAIL OF TWO CYCLES OF Fig. 1 (ref. waveform "1010" in Fig. 1)

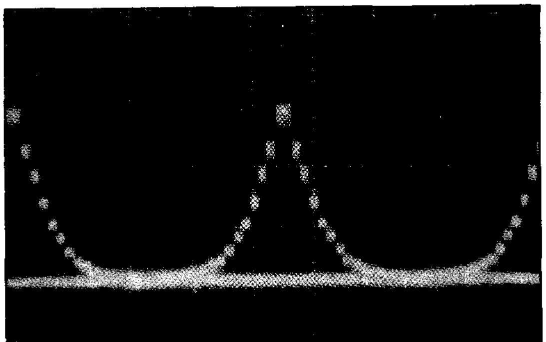


Fig. 4 SINGLE TONE WITH ENVELOPE SHAPE/CYCLE PATTERN 1010

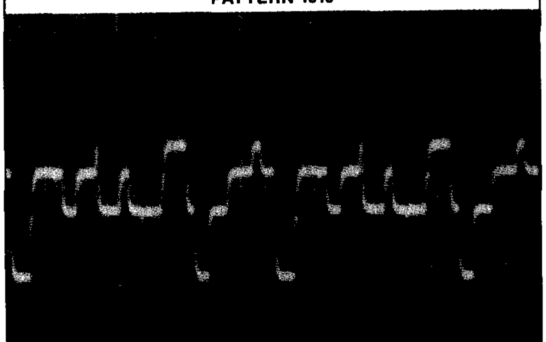


Fig. 5 MIXTURE OF THREE TONES WITH FIXED AMPLITUDES

AUDIO

I/O Port Data Store
(Registers R16, R17)

Registers R16 and R17 function as intermediate data storage registers between the PSG/CPU data bus (DA0--DA7) and the two I/O ports (IOA7--IOA0 and IOB7--IOB0). Both ports are available in the AY-3-8910; only I/O Port A is available in the AY-3-8912; none are available on the AY-3-8913. Using registers R16 and R17 for the transfer of I/O data has no effect on sound generation.

D/A Converter Operation

Since the primary use of the PSG is to produce sound for the highly imperfect amplitude detection mechanism of the human ear, the D/A conversion is performed in logarithmic steps with a normalized voltage range of from 0 to 1 Volt. The specific amplitude control of each of the three D/A Converters is accomplished by the three sets of 4-bit outputs of the Amplitude Control block, while the Mixer outputs provide the base signal frequency (Noise and/or Tone).

ELECTRICAL CHARACTERISTICS (AY-3-8910, AY-3-8912)

Maximum Ratings*

Storage Temperature . . . . −55° C to +150° C
Operating Temperature . . . . 0° C to +40° C
V_{CC} and all other Input/Output
Voltages with Respect to V_{SS} . . . . −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0° C to +40° C

Characteristics	Sym	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS						
All Inputs						
Low Level	V_{IL}	0	—	0.6	V	
High Level	V_{IH}	2.4	—	V_{CC}	V	
All Outputs (except Analog Channel Outputs)						
Low Level	V_{OL}	0	—	0.5	V	I_{OL} = 1.6mA, 20pf
High Level	V_{OH}	2.4	—	V_{CC}	V	I_{OH} = 100μA, 20pf
Analog Channel Outputs	V_o	0	—	60	dB	Test Circuit: Fig. 6
Power Supply Current	I_{CC}	—	45	85	mA	
AC CHARACTERISTICS						
Clock Input						
Frequency	f_C	1	—	2	MHz	Fig. 7
Rise Time	t_r	—	—	50	ns	Fig. 7
Fall Time	t_f	—	—	50	ns	Fig. 7
Duty Cycle	—	25	50	85	%	Fig. 7
Bus Signals (BDIR, BC2, BC1)						
Associative Delay Time	t_{BD}	—	—	50	ns	Fig. 7
Reset						
Reset Pulse Width	t_{RW}	500	—	—	ns	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	—	ns	Fig. 8
A9, A8, DA7--DA0 (Address Mode)						
Address Setup Time	t_{AS}	400	—	—	ns	Fig. 9
Address Hold Time	t_{AH}	100	—	—	ns	Fig. 9
DA7--DA0 (Write Mode)						
Write Data Pulse Width	t_{DW}	500	—	10,000	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	—	ns	Fig. 10
Write Data Hold Time	t_{DH}	100	—	—	ns	Fig. 10
DA7--DA0 (Read Mode)						
Read Data Access Time	t_{DA}	—	250	500	ns	Fig. 11
DA7--DA0 (Inactive Mode)						
Tristate Delay Time	t_{TS}	—	100	200	ns	Fig. 11

**Typical values are at +25° C and nominal voltages.

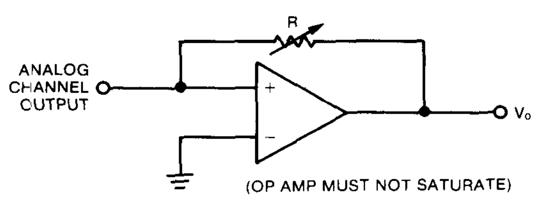


Fig. 6 ANALOG CHANNEL OUTPUT TEST CIRCUIT

AUDIO

ELECTRICAL CHARACTERISTICS (AY-3-8913)

Maximum Ratings*

Storage Temperature .... −55° C to +150° C
Operating Temperature .... 0° C to +70° C
V_{CC} and all other Input/Output Voltages
with Respect to V_{SS} .... −0.3V to +8.0V

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied—operating ranges are specified in Standard Conditions. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed.

Standard Conditions (unless otherwise noted):

V_{CC} = +5V ±5%
V_{SS} = GND
Operating Temperature = 0° C to +70° C

Characteristics	Sym	Min	Max	Units	Conditions
DC CHARACTERISTICS					
Input Voltage Levels					
Low Level	V_{IL}	0	0.7	V	
High Level	V_{IH}	2.2	V_{CC}	V	
Output Voltage Levels (except Analog Channel Outputs)					
Low Level	V_{OL}	0	0.4	V	1 TTL Load
High Level	V_{OH}	2.4	V_{CC}	V	+100pf
Analog Channel Outputs	V_O	0	2000	μA	Test Circuit: Fig. 6
Power Supply Current	I_{CC}	—	85	mA	
AC CHARACTERISTICS					
Clock Input					
Frequency	f_c	1	2.5	MHz	Fig. 7
Rise Time	t_r	—	50	ns	Fig. 7
Fall Time	t_f	—	50	ns	Fig. 7
Duty Cycle	—	40	60	%	Fig. 7
Bus Signals (BDIR, BC2, BC1)					
Associative Delay Time	t_{BD}	—	50	ns	Fig. 7
Reset					
Reset Pulse Width	t_{RW}	5	—	μs	Fig. 8
Reset to Bus Control Delay Time	t_{RB}	100	—	ns	Fig. 8
A9, A8, DA7--DA0 (Address Mode)					
Address Setup Time	t_{AS}	300	—	ns	Fig. 9
Address Hold Time	t_{AH}	50	—	ns	Fig. 9
DA7--DA0 (Write Mode)					
Write Data Pulse Width	t_{DW}	1800	—	ns	Fig. 10
Write Data Setup Time	t_{DS}	50	—	ns	Fig. 10
Write Data Hold Time	t_{DH}	100	—	ns	Fig. 10
DA7--DA0 (Read Mode)					
Read Data Access Time	t_{DA}	—	350	ns	Fig. 11
DA7--DA0 (Inactive Mode)					
Tristate Delay Time	t_{TS}	—	400	ns	Fig. 11

AUDIO

TIMING DIAGRAMS

Fig. 7 CLOCK AND BUS SIGNAL TIMING

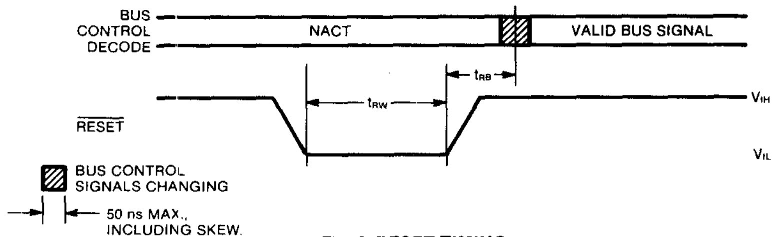
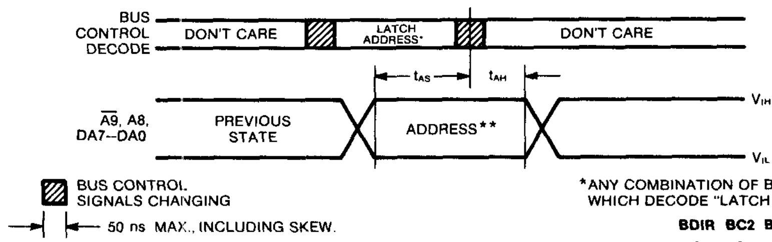


Fig. 8 RESET TIMING

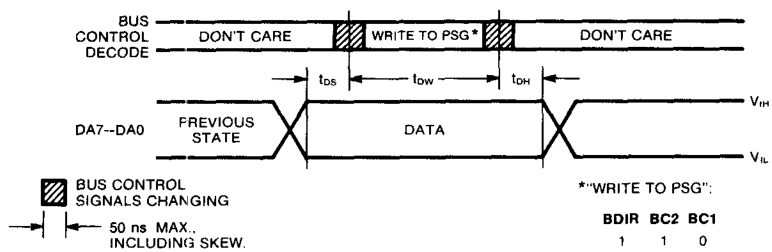


**REFER TO PARAGRAPH 2.1.1 FOR A DESCRIPTION OF "VALID" PSG ADDRESSING.

*ANY COMBINATION OF BDIR, BC2, BC1 WHICH DECODE "LATCH ADDRESS":

	BDIR	BC2	BC1
	0	0	1
or	1	0	0
or	1	1	1

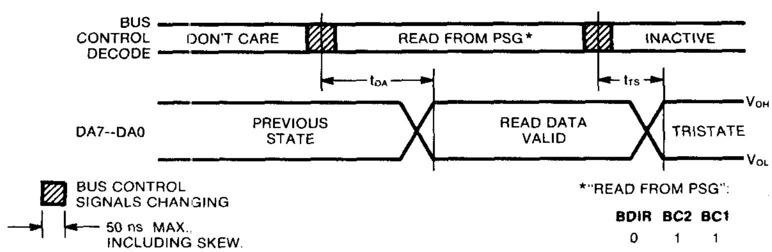
Fig. 9 LATCH ADDRESS TIMING



*"WRITE TO PSG":

BDIR	BC2	BC1
1	1	0

Fig. 10 WRITE DATA TIMING



*"READ FROM PSG":

BDIR	BC2	BC1
0	1	1

Fig. 11 READ DATA TIMING

AUDIO

Programable Sound Generator

FEATURES

- Full software control of sound generation
- Interfaces to most 8-bit and 16-bit microprocessors
- Three independently programed analog outputs
- Two 8-bit general purpose I/O ports (AY-3-8910)
- One 8-bit general purpose I/O port (AY-3-8912)
- Single +5V Supply

DESCRIPTION

The AY-3-8910/8912/8913 Programable Sound Generator (PSG) is a Large Scale Integrated Circuit which can produce a wide variety of complex sounds under software control. The AY-3-8910/8912/8913 is manufactured in the General Instrument N-Channel Ion Implant Process. Operation requires a single 5V power supply, a TTL compatible clock, and a microprocessor controller such as the General Instrument 16-bit CP1600/1610 or one of the General Instrument PIC1650 series of 8-bit microcomputers.

The PSG is easily interfaced to any bus oriented system. Its flexibility makes it useful in applications such as music synthesis, sound effects generation, audible alarms, tone signalling and FSK modems. The analog sound outputs can each provide 4 bits of logarithmic digital to analog conversion greatly enhancing the dynamic range of the sounds produced.

In order to perform sound effects while allowing the processor to continue its other tasks, the PSG can continue to produce sound after the initial commands have been given by the control processor. The fact that realistic sound production often involves more than one effect is satisfied by the three independently controllable channels available in the PSG.

All of the circuit control signals are digital in nature and intended to be provided directly by a microprocessor/microcomputer. This means that one PSG can produce the full range of required sounds with no change in external circuitry. Since the frequency response of the PSG ranges from sub-audible at its lowest frequency to post-audible at its highest frequency, there are few sounds which are beyond reproduction with only the simplest electrical connections.

Since most applications of a microprocessor/PSG system would also require interfacing between the outside world and the microprocessor, this facility has been designed into the PSG. The AY-3-8910 has two general purpose 8-bit I/O ports and is supplied in a 40 lead package; the AY-3-8912 has one port and 28 leads: the AY-3-8913 has no I/O ports and 24 leads.

See complete data sheets of AY-3-8910/8912/8913 in Audio Section.

PIN CONFIGURATION

40 LEAD DUAL IN LINE
AY-3-8910

Top View

V_{SS} (GND)	1	40	V_{CC} (+5V)
N.C.	2	39	TEST 1
ANALOG CHANNEL B	3	38	ANALOG CHANNEL C
ANALOG CHANNEL A	4	37	DA0
N.C.	5	36	DA1
IOB7	6	35	DA2
IOB6	7	34	DA3
IOB5	8	33	DA4
IOB4	9	32	DA5
IOB3	10	31	DA6
IOB2	11	30	DA7
IOB1	12	29	BC1
IOB0	13	28	BC2
IOA7	14	27	BDIR
IOA6	15	26	TEST 2
IOA5	16	25	A8
IOA4	17	24	$\overline{A9}$
IOA3	18	23	$\overline{RESET}$
IOA2	19	22	CLOCK
IOA1	20	21	IOA0

28 LEAD DUAL IN LINE
AY-3-8912

Top View

ANALOG CHANNEL C	1	28	DA0
TEST 1	2	27	DA1
V_{CC} (+5V)	3	26	DA2
ANALOG CHANNEL B	4	25	DA3
ANALOG CHANNEL A	5	24	DA4
V_{SS} (GND)	6	23	DA5
IOA7	7	22	DA6
IOA6	8	21	DA7
IOA5	9	20	BC1
IOA4	10	19	BC2
IOA3	11	18	BDIR
IOA2	12	17	A8
IOA1	13	16	$\overline{RESET}$
IOA0	14	15	CLOCK