

STANDARD VGA REGISTERS

(Based on a document provided by Oak Technologies)

VGA REGISTERS INDEX	1
GENERAL REGISTERS	4
MISCELLANEOUS OUTPUT REGISTER	4
INPUT STATUS REGISTER 0	5
INPUT STATUS REGISTER 1	6
FEATURE CONTROL REGISTER	7
DAC REGISTERS	7
SEQUENCER REGISTERS	8
SEQUENCER ADDRESS REGISTER	8
RESET REGISTER	8
CLOCKING MODE REGISTER	9
MAP MASK REGISTER	10
CHARACTER MAP SELECT REGISTER	10
MEMORY MODE REGISTER	12
CRT CONTROLLER REGISTERS	13
CRT CONTROLLER ADDRESS REGISTER	13
HORIZONTAL TOTAL REGISTER	13
HORIZONTAL DISPLAY ENABLE END REGISTER	13
START HORIZONTAL BLANKING REGISTER	14
END HORIZONTAL BLANKING REGISTER	14
START HORIZONTAL RETRACE PULSE REGISTER	15
PRESET ROW SCAN REGISTER	15
MAXIMUM SCAN LINE REGISTER	16
CURSOR START REGISTER	16
CURSOR END REGISTER	16
START ADDRESS HIGH REGISTER	17
START ADDRESS LOW REGISTER	17
CURSOR LOCATION HIGH REGISTER	17
CURSOR LOCATION LOW REGISTER	17
VERTICAL RETRACE START REGISTER	18
VERTICAL RETRACE END REGISTER	18
VERTICAL DISPLAY ENABLE END REGISTER	19
OFFSET REGISTER	19
UNDER LINE LOCATION REGISTER	19
START VERTICAL BLANKING REGISTER	20
END VERTICAL BLANKING REGISTER	20
CRTC MODE CONTROL REGISTER	20
LINE COMPARE REGISTER	22
GRAPHICS CONTROLLER REGISTERS	23
GRAPHICS ADDRESS REGISTER	23
SET/RESET REGISTER	23
ENABLE SET/RESET REGISTER	23
COLOR COMPARE REGISTER	23

DATA ROTATE REGISTER	24
READ MAP SELECT REGISTER	24
GRAPHICS MODE REGISTER	25
MISCELLANEOUS REGISTER	26
COLOR DON'T CARE REGISTER	27
ATTRIBUTE CONTROLLER REGISTER	28
ATTRIBUTE ADDRESS REGISTER	28
PALETTE REGISTERS HEX 00 THROUGH OF	28
ATTRIBUTE MODE CONTROL REGISTER	29
OVERSCAN COLOR REGISTER	30
COLOR PLANE ENABLE REGISTER	30

VGA REGISTERS INDEX

GENERAL

These registers control the overall activity of the VGA controller.

<u>Register</u>	<u>R/W</u>	<u>Mono Port</u>	<u>Color Port</u>	<u>Index</u>
Miscellaneous Output	W	3CC/3C2	3CC/3C2	
Input Status 0	R	3C2	3C2	
Input Status 1	R	3BA	3DA	
Feature Control	R/W	3CA/3BA	3CA/3DA	
DAC State	R	03C7	03C7	

SEQUENCER

The sequencer controls basic aspects of the clocks that feed into the VGA controller.

<u>Register</u>	<u>R/W</u>	<u>Mono Port</u>	<u>Color Port</u>	<u>Index</u>
Sequencer Address	R/W	3C4	3C4	
Reset	R/W	3C5	3C5	00
Clocking Mode	R/W	3C5	3C5	01
Plane Mask	R/W	3C5	3C5	02
Character Map Select	R/W	3C5	3C5	03
Memory Mode	R/W	3C5	3C5	04

GRAPHICS CONTROLLER

The graphics controller settings control how the system processor reads and writes to and from video memory.

<u>Register</u>	<u>R/W</u>	<u>Mono Port</u>	<u>Color Port</u>	<u>Index</u>
Graphics Controller Index	R/W	3CE	3CE	
Set/Reset	R/W	3CF	3CF	00
Enable Set/Reset	R/W	3CF	3CF	01
Color Compare	R/W	3CF	3CF	02
DataRotate	R/W	3CF	3CF	03

Read Map Select	R/W	3CF	3CF	04
Mode	R/W	3CF	3CF	06
Miscellaneous	R/W	3CF	3CF	06
Color Don't Care	R/W	3CF	3CF	07
Bit Mask	R/W	3CF	3CF	08

ATTRIBUTE CONTROLLER

These registers are the original CGA/EGA palette and border color registers. They are pretty much obsolete, except for text modes.

<u>Register</u>	<u>R/W</u>	<u>Mono Port</u>	<u>Color Port</u>	<u>Index</u>
Attribute Controller Index	R/W	3C0	3C0	
Color Palette Register 0-15	R/W	3C0	3C0	00-0F
Mode Control	R/W	3C0	3C0	10
Overscan Control	R/W	3C0	3C0	11
Color Plane Enable	R/W	3C0	3C0	12
Horizontal Pixel Panning	R/W	3C0	3C0	13
Color Select	R/W	3C0	3C0	14

CRT CONTROLLER

This block of registers controls the various counters that are used to generate the video timing signals (VSYNC, HSYNC, BLANK, etc) and for clocking out video data.

<u>Register</u>	<u>R/W</u>	<u>Mono Port</u>	<u>Color Port</u>	<u>Index</u>
CRTC Address	R/W	3B4	3D4	
Horizontal Total	R/W	3B5	3B5	00
Horizontal Display Enable End	R/W	3B5	3D5	01
Start Horizontal Blanking	R/W	3B5	3D5	02
End Horizontal Blanking	R/W	3B5	3D5	03
Start Horizontal Retrace Pulse	R/W	3B5	3D5	04
End Horizontal Retrace	R/W	3B5	3D5	05
Vertical Total	R/W	3B5	3D5	06
Overflow	R/W	3B5	3D5	07
Preset Row Scan	R/W	3B5	3D5	08
Maximum Scan Line	R/W	3B5	3D5	09
Cursor Start	R/W	3B5	3D5	0A
Cursor End	R/W	3B5	3D5	0B
Start Address High	R/W	385	3D5	0C
Start Address Low	R/W	3B5	3D5	0D
Cursor Location High	R/W	3B5	3D5	0E

Cursor Location Low	R/W	3B5	3D5	OF
Vertical Retrace Start	W	3B5	3D5	10
Vertical Retrace End	W	3B5	3D5	11
Vertical Display Enable End Offset	R/W	3B5	3D5	12
Underline Location	R/W	3B5	3D5	13
Start Vertical Blanking	R/W	3B5	3D5	14
End Vertical Blanking	R/W	3B5	3D5	15
CRTC Mode Control	R/W	3B5	3D5	16
Line Comparator Register	R/W	3B5	3D5	17
Read-back CRT Latches	R	3B5	3D5	18
Attribute Index Toggle	R	3B5	3D5	22
Attribute Index Register	R/W	3B5	3D5	24
				23

GENERAL REGISTERS

MISCELLANEOUS OUTPUT REGISTER

Read address = 3CC hex; Write address 3C2 hex

- | <u>Bit</u> | <u>Description</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|------------|--|------------|----------------------------------|------------|--------------|---|---|---|------------|---|---|---|------------|---|---|---|--------|---|---|---|----------|---|---|---|----------------------------------|---|---|---|------------------------------|---|---|---|--------|---|---|---|--------|
| 0 | Input/Output Address Select - This bit maps the CRTC I/O addresses for monochrome or color emulation.

0 = Monochrome emulation with CRTC addresses set to 3Bx hex, Input Status 1 register set to 3BA hex.
1 = Color emulation with CRTC addresses set to 3Dx, Input Status 1 register set to 3DA hex. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | Enable RAM
0 = Disable Video RAM address decode from the system microprocessor.

1 = Enable Video RAM to the system microprocessor. | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 2,3 | Clock Select - These two bits, CSEL0 and CSEL1, are used with 3DF index D bit 5 as follows:

<table><thead><tr><th><u>CS2</u></th><th><u>CS1</u></th><th><u>CS0</u></th><th><u>Clock</u></th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td><td>25.175 MHz</td></tr><tr><td>0</td><td>0</td><td>1</td><td>28.322 MHz</td></tr><tr><td>0</td><td>1</td><td>0</td><td>65 MHz</td></tr><tr><td>0</td><td>1</td><td>1</td><td>44.9 MHz</td></tr><tr><td>1</td><td>0</td><td>0</td><td>14.161 MHz (derived from 28.322)</td></tr><tr><td>1</td><td>0</td><td>1</td><td>18 MHz (derived from 36 MHz)</td></tr><tr><td>1</td><td>1</td><td>0</td><td>40 MHz</td></tr><tr><td>1</td><td>1</td><td>1</td><td>36 MHz</td></tr></tbody></table>
(These bits have been overridden by the Oak Extended Register 06. Any bits written here must be the same as those written to Extended Register 06). | <u>CS2</u> | <u>CS1</u> | <u>CS0</u> | <u>Clock</u> | 0 | 0 | 0 | 25.175 MHz | 0 | 0 | 1 | 28.322 MHz | 0 | 1 | 0 | 65 MHz | 0 | 1 | 1 | 44.9 MHz | 1 | 0 | 0 | 14.161 MHz (derived from 28.322) | 1 | 0 | 1 | 18 MHz (derived from 36 MHz) | 1 | 1 | 0 | 40 MHz | 1 | 1 | 1 | 36 MHz |
| <u>CS2</u> | <u>CS1</u> | <u>CS0</u> | <u>Clock</u> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 0 | 25.175 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 0 | 1 | 28.322 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 0 | 65 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 1 | 44.9 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 0 | 14.161 MHz (derived from 28.322) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 0 | 1 | 18 MHz (derived from 36 MHz) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 0 | 40 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 1 | 1 | 1 | 36 MHz | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 4 | Reserved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5 | Page Bit For Odd/Even - Select between two pages of memory when in the odd or even modes (0-5). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

- 0 - Low 64K page of memory
- 1 - High 64K page of memory
- 6 Horizontal Sync Polarity
 - 0 - Positive Vertical Retrace
 - 1 - Negative Vertical Retrace
- 7 Vertical Sync Polarity
 - 0- Positive Vertical Retrace
 - 1- Negative Vertical Retrace

Bits 6 and 7 are used to select the vertical size of the monitor as follows:

<u>Bit7</u>	<u>Bit6</u>	
0	0	Reserved
0	1	400 lines
1	0	350 lines
1	1	480 lines

INPUT STATUS REGISTER 0

Read address = 3C2 hex

<u>Bit</u>	<u>Description</u>
------------	--------------------

0-3	Reserved
-----	----------

- | | |
|---|---|
| 4 | Switch Sense Bit • Reports the status of one of the four switches selected via the clock select to the Miscellaneous Output register. This bit allows the power-on initialization to determine if a monochrome or color monitor is connected to the system. |
|---|---|

0 - Selected sense switch is off or 0.

1 - Selected sense switch is on or 1.

5,6	Reserved
-----	----------

7 CRT interrupt

0 = Vertical retrace interrupt is pending

1 = Vertical retrace Interrupt is cleared.

INPUT STATUS REGISTER 1

Read address = 3BA/3DA hex

Bit Description

0 Display Enable = Monitors the status of the display. To avoid glitches on the display, some programs watch this bit to restrict screen updates to inactive display periods. The VGA has been designed to eliminate this requirement, so display screen updates may be made at any time.

0 - The display of video data is enabled.

1 - The display is in horizontal or vertical retrace mode.

1,2 Reserved

3 Vertical Retrace

0 - Video information Is being displayed.

1 - A vertical retrace interval is in progress.

4,5 Diagnostic Usage - reports the status of two of the VGA attribute controller outputs. The values set Into the Video status MUX field of the Color Plans Enable register determine which colors are input to these two diagnostic bits.

Color Plane Register

Bit 5 Bit 4

0 0

0 1

1 0

1 1

Input Status Register 1

Bit 5 Bit 4

P2 P0

P5 P4

P3 P1

P7 P6

6,7 Reserved

FEATURE CONTROL REGISTER

Read address = 3CA hex; Write address = 3BA/3DA hex

<u>Bit</u>	<u>Description</u>
0-2	Reserved
3	Vertical Sync Select 0 - This bit should always be set to 0 to enable normal Vertical Sync output to the monitor 1 - The Vertical Sync output is the logical OR of vertical Sync end Vertical display enable.
4-7	Reserved

DAC REGISTERS

PEL Mask	R/W	3C6
DAC State Register	R	3C7
PEL Address (Read Mode)	W	3C7
PEL Address (Write Mode)	R/W	3C8
PEL Data Register	R/W	3C9

SEQUENCER REGISTERS

SEQUENCER ADDRESS REGISTER

Port address - 3C4 hex

This register is a pointer register located at address 03C4 hex. It is loaded with a binary value that points to the SEQUENCER Data register where data is to be written. This value is referred to as the Index.

<u>Bit</u>	<u>Description</u>
0-2	Sequencer Address bits - A binary value pointing to the register where data is to be read or written.
3-7	Reserved

RESET REGISTER

Port address = 3C5 hex, Index 00 hex

This Is a read/write register pointed to when the value in the Sequencer Address register is 00 hex.

<u>Bit</u>	<u>Description</u>
0	Asynchronous Reset - This bit, synchronous reset, or both should be set to 0 before changing bit 0 or bit 3 of the Clocking Mode register or bit 2 or bit 3 of the Miscellaneous Output register, or all bits of register 3DF index D. 0 - Asynchronous clear and halt the sequencer. This may cause data loss In the dynamic RAM's. 1 - Bit 1 and 0 must be 1 to allow the sequencer to operate.
1	Synchronous Reset This bit, asynchronous reset, or both should be set to 0 before changing bit 0 or bit 3 of the Clocking Mode register or bit 2 or bit 3 of the Miscellaneous Output register, or all bits of register 3DF index D. 0 - Synchronous clear and halt the sequencer.

1 - Bit 1 and 0 must be 1 to allow the sequencer to operate.

2-7 Reserved

CLOCKING MODE REGISTER

Port address = 03C5 hex; Index 01 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 01 hex.

<u>Bit</u>	<u>Description</u>
0	8/9 Dot Clocks • The 9 dot mode Is for Alphanumeric modes only. The ninth dot equals the eighth dot for ASCII codes C0 through DF hex. Also see the Line Graphics Character Code bit in the Attribute Mode Control register section. 0 - Directs the sequencer to generate nine dot wide character clocks. 1 - Generate eight dot wide character clocks.
1	Reserved
2	Shift Load 0 - If bit 4 Is set to 0, also, the video serializers are reloaded every character clock. 1 - The video serializers are reloaded every other character clock. this mode is useful when 16 bits are fetched per cycle and chained together In the shift load registers.
3	Dot clock - All other timings will be affected since they are derived from the dot dock. 0 - Select normal dot docks derived from the sequencer master clock Input. 1 - The master clock will be divided by 2 to generate the dot clock. This is used for 320 and 360 horizontal PEL modes.

4 Shift 4

0 - The video serializers are reloaded every character clock.

1 - The serializers are loaded every fourth character clock This is useful when 32 bits are fetched per cycle and chained together in the shift registers.

5 Screen Off - This bit is used for fast full-screen updates.

0 = Normal screen operation.

1 = Turns off the video screen and assigns the maximum memory bandwidth to the system CPU.

6,7 Reserved

MAP MASK REGISTER

Port address = 3C5 hex; index 02 hex

This is a read/write register pointed to when the Sequencer Address register is 02 hex.

<u>Bit</u>	<u>Description</u>
------------	--------------------

0-3	Map Mask - For odd/even modes, maps 0 and 1, and maps 2 and 3 should have the same map mask value. When chain 4 mode is selected, all maps should be enabled. This is a read-modify-write operation.
-----	--

0 = Disable memory write to the corresponding map.

1 = Enables the system to write to the corresponding map. If all four bits are set to 1, the system CPU can perform a 32-bit operation with only one memory cycle.

4-7 Reserved

CHARACTER MAP SELECT REGISTER

Port address = 3C5 hex; index 03 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 03 hex.

Bit **Description**
 0,1 Character Map Select B - Selects the portion of map 2 used to generate Alpha characters with bit 4 as the high bit when attribute bit 3 is 0.

<u>Bit4</u>	<u>Bit1</u>	<u>Bit0</u>	<u>Map</u>	<u>Table location</u>
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2
1	1	1	7	8th 8k of Map 2

2,3 Character Map Select A - Select the portion of map 2 used to generate Alpha characters with bit 5 as the high bit when attribute bit 3 is 1. Bit 3 of the attribute byte normally controls the ON/OFF of the foreground intensity in text modes. This bit may be redefined as a switch between character sets. For this feature to be enabled, the following statements must be true:

- * The setting value of Character Map Select A does not equal the value of Character Map Select B.
- * The Memory Mode register bit 1, must be equal to 1.

If either of these are not true, the first 16K of Map 2 is used.

<u>Bit5</u>	<u>Bit3</u>	<u>Bit2</u>	<u>Map</u>	<u>Table Location</u>
0	0	0	0	1st 8k of Map 2
0	0	1	1	3rd 8k of Map 2
0	1	0	2	5th 8k of Map 2
0	1	1	3	7th 8k of Map 2
1	0	0	4	2nd 8k of Map 2
1	0	1	5	4th 8k of Map 2
1	1	0	6	6th 8k of Map 2

	1	1	1	7	8th 8k of Map 2
4	Character Map Select High Bit B				
5	Character Map Select High Bit A				
6,7	Reserved				

MEMORY MODE REGISTER

Port address = 3C5 hex; index 04 hex

This is a read/write register pointed to when the value in the Sequencer Address register is 04 hex

<u>Bit</u>	<u>Description</u>
0	Reserved
1	Extended memory 0 = No extended memory present. Display memory is less than 64 Kbytes. 1 = Extended memory is present. Display memory is greater than 64 Kbytes. If set to 1 the VGA is configured to use 256k bytes of video memory. This also enables character map selection.
2	Odd/Even 0 = Directs even CPU addresses to access maps 0 and 2, and odd CPU addresses to access maps 1 and 3. 1 = If bit 3 is set to 0, this bit causes system CPU addresses to sequentially address data within a bit map.
3	Chain 4 0 = If bit 2 is set to 1, this bit enables the system CPU to address data sequentially within a bit map by use of the Map Mask register. 1 = Causes two low-order address bits to select the map that will be accessed as follows:

<u>A1</u>	<u>A0</u>	<u>Map Selected</u>
0	0	0
0	1	1
1	0	2
1	1	3

4-7 Reserved

CRT CONTROLLER REGISTERS

CRT CONTROLLER ADDRESS REGISTER

Port address = 3B4/3D4 hex

This register is a pointer register located at 3B4 hex for Monochrome emulation modes or 3D4 hex for Color emulation modes depending on bit 0 of the Miscellaneous output register at address 3C2 hex. The CRT Controller Addresses register is loaded with a binary value, or index, that points to the CRT Controller Data register where data is to be Written. All CRT controller registers are read/write registers.

<u>Bit</u>	<u>Description</u>
0-4	CRT Controller Address Bits - A binary value programmed in these bits selects one of the CRT Controller registers where data is to accessed.
5	Test Bit - Must remain 0.
6,7	Reserved

HORIZONTAL TOTAL REGISTER

Port address = 3B5/3D5 hex; index = 00 hex

<u>Bit</u>	<u>Description</u>
0-7	Horizontal Total This register defines the total number of characters in the horizontal interval including the retrace time. This value directly controls the period of the horizontal retrace output signal. Character clock inputs to the CRT controller and counted by an international horizontal character counter. This value is compared with the horizontal character values to provide horizontal timings. All horizontal and vertical timings are based upon the horizontal register. The value programmed is 5 less than the desired value.

HORIZONTAL DISPLAY ENABLE END REGISTER

Port address = 3B5/3D5 hex; index = 01 hex

<u>Bit</u>	<u>Description</u>
0-7	Horizontal Display Enable End - The total number of displayed characters minus 1. This register defines the length of the horizontal display enable signal. It determines the number of displayed characters per horizontal line.

START HORIZONTAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 02 hex

<u>Bit</u>	<u>Description</u>
0-7	Start horizontal blanking - Determines when to start the internal horizontal blanking output signal. When the internal character counter reaches this value, the horizontal blanking signal becomes active.

END HORIZONTAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 03 hex

This register determines when the horizontal blanking output signal becomes inactive.

<u>Bit</u>	<u>Description</u>
0-4	End Horizontal Blanking - The horizontal blanking signal width is determined as follows: Value of Start Blanking register + width of blanking signal in character clock units =6-bit result to be programmed into the End Horizontal blanking register. Bit number 5 is located in the End Horizontal Retrace register. If these six bits equal the six least significant bits the horizontal character counter, the horizontal blanking signal becomes inactive.

5,6 Display Enable Skew Control - These two bits indicate the magnitude of display enable skew. Bits 5 and 6 and the amount of skew are as follows:

<u>Bit6</u>	<u>Bit5</u>	<u>Skew</u>
0	0	Zero character clock skew
0	1	One character clock skew
1	0	Two character clock skew
1	1	Three character clock skew
7		Test Bit - Must be set to 1

START HORIZONTAL RETRACE PULSE REGISTER

Port address = 3B5/3D5 hex; index = 05 hex

This register specifies the character position at which the Horizontal Retrace Pulse becomes inactive.

<u>Bit</u>	<u>Description</u>
0-4	End horizontal Retrace - The value programmed here is compared to the five least-significant bits of the horizontal character counter. When they are equal, the horizontal retrace signal becomes inactive (logical 0). To calculate the width of the retrace signal use the following algorithm: Value of Start Horizontal Retrace register + width of Horizontal Retrace signal in character in clock units = 5-bit result to be programmed into the End Horizontal Retrace register.

PRESET ROW SCAN REGISTER

Port address = 3B5/3D5 hex; index = 08 hex

<u>Bit</u>	<u>Description</u>
0-4	Preset Row Scan (PEL Scrolling) - These bits specify the starting row scan counter after a vertical retrace. The row scan counter increments each horizontal retrace time until a maximum row scan occurs. At maximum row scan compare time, the scan is cleared (not preset).
5,6	Byte Panning Control - This field controls byte panning in modes programmed as multiple shift modes, which is required for PEL-panning operations. The Horizontal PEL Panning register in the Attribute Controller provides panning of up to 8 individual PEL-panning operations. In single byte shift modes, the CRT Controller start address is incremented and attribute panning is reset to 0 to pan to the next higher PEL. In multiple shift modes, the byte pan bits are used as extensions to the attribute PEL Panning register. This allows panning across the width of the video output shift.
7	Reserved

MAXIMUM SCAN LINE REGISTER

Port address = 3B5/3D5 hex; index = 09 hex

<u>Bit</u>	<u>Description</u>
0-4	Maximum Scan Line - These bits specify the number of scan lines per character row. The number to be programmed is the maximum row number minus 1.
5	Start Vertical Blank - Bit 9 of the Start Vertical Blank Register (index 15 hex).
6	Line Compare - Bit 9 of the Line Compare Register (index 18 hex).
7	200 to 400 Line Conversion - 0 = The clock to the row scan counter is equal to the horizontal scan rate. Line doubling is disabled. 1 = The clock in the row scan counter is divided by 2. This allows the older 200-line modes to be displayed as 400 lines on the display. This is referred to as line doubling.

CURSOR START REGISTER

Port address = 3B5/3D5 hex; index = 0A hex

If the Cursor Start register is programmed with a value greater than the cursor End register, no cursor is generated.

<u>Bit</u>	<u>Description</u>
0-4	Cursor Start - This field specifies the row scan line of a character line where the cursor is to begin.
5	Cursor Off 0 = Turns On the Cursor 1 = Turns Off the Cursor
6,7	Reserved

CURSOR END REGISTER

Port address = 3B5/3D5 hex; index = 0B hex

<u>Bit</u>	<u>Description</u>
0-4	Cursor End - This field specifies the row scan of a character line where the cursor is to end.

- 5,6 Cursor Skew - These bits control the skew of the cursor signal. Cursor skew delays the cursor by the number of clocks.

<u>Bit6</u>	<u>Bit5</u>	<u>Function</u>
0	0	Zero-character clock skew
0	1	One-character clock skew
1	0	Two-character clock skew
1	1	Three-character clock skew

- 7 Reserved.

START ADDRESS HIGH REGISTER

Port address = 3B5/3D5 hex; index 0C hex

<u>Bit</u>	<u>Description</u>
0-7	Start Address High - This register contains the high-order 8-bits of the start address. The 16-bit value, from the high-order and low-order Start Address registers, is the first address after the vertical retrace on each screen refresh.

START ADDRESS LOW REGISTER

Port address = 3B5/3D5 hex; index = 0D hex

<u>Bit</u>	<u>Description</u>
0-7	Start Address Low - This register contains the low-order 8-bits of the start address.

CURSOR LOCATION HIGH REGISTER

Port address = 3B5/3D5 hex; index = 0E hex

<u>Bit</u>	<u>Description</u>
0-7	Cursor High - This register contains the high-order 8-bits of the cursor location.

CURSOR LOCATION LOW REGISTER

Port address = 3B5/3D5 hex; index = 0F hex

<u>Bit</u>	<u>Description</u>
0-7	Cursor Low - This register contains the low-order 8-bits of the cursor location.

VERTICAL RETRACE START REGISTER

Port address = 3B5/3D5 hex; index = 10 hex

<u>Bit</u>	<u>Description</u>
0-7	Vertical Retrace Start - This register contains the low-order 8-bits of the vertical retrace pulse start position, Programmed in horizontal scan lines. Bit 8 and 9 are in the CRTC Overflow register (index 07 hex).

VERTICAL RETRACE END REGISTER

Port address = 3B5/3D5 hex; index = 11 hex

<u>Bit</u>	<u>Description</u>
0-3	Vertical Retrace End - This field determines the horizontal scan count value when the vertical retrace output signal becomes inactive. This register is programmed in units of horizontal scan lines. To obtain a vertical retrace signal of width W, use the following algorithm: Value of Start Vertical Retrace register + width of vertical retrace signal in horizontal Retrace register = 4-bit result to be programmed into the End Vertical Retrace register.
4	Clear Vertical Interrupt 0 = Clears the vertical retrace interrupt flip-flop 1 = Allows the vertical interrupt to be set at the start of the next vertical retrace interval.
5	Enable Vertical Interrupt 0 = Enables a vertical retrace interrupt (on IRQ2). This interrupt level may be shared so the input Status register 0, bit 7 should be checked to find out if the VGA caused the interrupt to occur. 1 = Disable vertical retrace interrupt.

- 6 **Select 5 Refresh Cycles**
0 = Selects three refresh cycles. The BIOS sets this bit to 0 during a mode set, a reset, or power on.
1 = Selects five refresh cycles per horizontal line. This allows the use of the VGA chip with slow sweep rate displays (15.75 KHz).
- 7 **Protect RO-7**
0 = Enables writing to CRTC registers 0-7.
1 = Disables writing to CRTC registers 0-7. The line compare bit 4 in register 07 hex is not protected.

VERTICAL DISPLAY ENABLE END REGISTER

Port address = 3B/3D5 hex; index = 12 hex

<u>Bit</u>	<u>Description</u>
0-7	Vertical Display Enable End - This register contains the low-order 8 bits of a 10-bit register that defines the vertical display enable end position. Bits 8 and 9 are located in the CRT Controller Overflow register 07 hex, bit 1 and 6, respectively.

OFFSET REGISTER

Port address = 3B5/3D5 hex; index = 13 hex

<u>Bit</u>	<u>Description</u>
0-7	Offset - This register specifies the logical line width of the screen. The starting memory address for the next character row is larger than the current character row by a factor of two or four times the Offset register contents.

UNDER LINE LOCATION REGISTER

Port address = 3B5/3D5 hex; index = 14 hex

<u>Bit</u>	<u>Description</u>
0-4	Underline Location - This field specifies the horizontal row scan of a character row on which an underline occurs. The value programmed is one less than the scan line number desired.

- 5 Count By 4
 - 0 = Normal clocking
 - 1 = The memory address counter is clocked with the character clock divided by 4.
- 6 Double-word Mode
 - 0 = Normal word addressing mode.
 - 1 = Memory addresses are double-word addresses.
- 7 Reserved

START VERTICAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 15 hex

<u>Bit</u>	<u>Description</u>
0-7	Start vertical blank - This register contains the low 8-bits of a 10-bit register. Bit 8 is in the CRTC Overflow register (index 07 hex). Bit 9 is in the Maximum Scan Line register (index 09 hex).

END VERTICAL BLANKING REGISTER

Port address = 3B5/3D5 hex; index = 16 hex

<u>Bit</u>	<u>Description</u>
0-7	End Vertical Blank - This register specifies the horizontal scan count value when the vertical blank output signal becomes inactive. It is programmed in units of horizontal scan lines. To obtain the vertical blank signal of width W, use the following algorithm: Value of Start Vertical Blank register minus 1 + width of vertical blank signal in horizontal scan units = 8-bit result to be programmed into the End Vertical Blank register.

CRTC MODE CONTROL REGISTER

Port address = 3B5/3D5 hex; index = 17 hex

<u>Bit</u>	<u>Description</u>
0	Compatibility Mode Support <ul style="list-style-type: none"> 0 = Row scan address bit 0 is substituted for memory address output bit 13 during active display time. 1 = Enables memory address bit 13 to appear on the memory address output bit 13 of the CRT controller.

- 1 **Select Row Scan Counter**
0 = Selects row scan counter bit 1 for CRT memory address bit MA14.
1 = Selects MA14 counter bit for CRT memory address bit MA14.

 - 2 **Horizontal Retrace Select**
0 = Selects normal horizontal retrace as the clock that controls the vertical timing counter.
1 = Selects horizontal retrace divided by 2 as the clock that controls the vertical timing counter. Therefore, the vertical resolution is doubled to 2048 horizontal scan lines.

 - 3 **Count By Two**
0 = The memory address counter is clocked with the character clock input.
1 = Clocks the memory address counter with the character clock input divided by 2.

 - 4 **Reserved**

 - 5 **Address Wrap - Selects memory address counter bit MA13 or bit MA15, and it appears on MA0 in word address mode. If the VGA is not in word address mode, MA0 counter output appears on MA0.**
0 = Selects MA13. This is selected in applications where only 64K memory is present.
1 = Selects MA15. This should be selected in odd/even mode since 256K of video memory is installed on the board.

 - 6 **Word Mode or Byte Mode - Bit 6 of the End Vertical Blanking register in the CRT Controller also controls the addressing. When it is set to 0, bit 6 of this register has control. When it is set to 1, the addressing is forced to be shifted by two bits.**
0 = The word mode shifts all memory address counter bits down one bit, and the most-significant bit of the counter appears on the least-significant bit of the memory address outputs.
1 = Selects the byte address mode.
- | | | | |
|--------|------|------|-------------|
| Memory | Byte | Word | Double-word |
|--------|------|------|-------------|

<u>Address</u>	<u>Address Mode</u>	<u>Address Mode</u>	<u>Address Mode</u>
MA0/RFA0	MA0	MA15 orMA13	MA12
MA1/RFA1	MA1	MA0	MA13
MA2/RFA2	MA2	MA1	MA0
MA3/RFA3	MA3	MA2	MA1
MA4/RFA4	MA4	MA3	MA2
MA5/RFA5	MA5	MA4	MA3
MA6/RFA6	MA6	MA5	MA4
MA7/RFA7	MA7	MA6	MA5
MA8/RFA8	MA8	MA7	MA6
MA9/RFA9	MA9	MA8	MA7
MA10	MA10	MA9	MA8
MA11	MA11	MA10	MA9
MA12	MA12	MA11	MA10
MA13	MA13	MA12	MA11
MA14	MA14	MA13	MA12
MA15	MA15	MA14	MA13

7 Hardware Reset

0 = Forces horizontal and vertical retrace to clear.

1 = Forces horizontal and vertical retrace to be enabled.

LINE COMPARE REGISTER

Port address = 3B5/3D5 hex; index = 18 hex

<u>Bit</u>	<u>Description</u>
0-7	Line Compare - This register is the low-order 8-bit of the compare target. When the vertical counter reaches this value, the internal start of line counter is cleared. Because of this, an area of the screen is not affected by scrolling. Bit 8 is located in the Overflow register 07 hex. Bit 9 is located in the Maximum Scan Line register 09 hex.

GRAPHICS CONTROLLER REGISTER

GRAPHICS ADDRESS REGISTER

Port address = 3CE hex

<u>Bit</u>	<u>Description</u>
0-3	Graphics Address Bits - These bits are used to point to the other registers in the graphics section.
4-7	Reserved

SET/RESET REGISTER

Port address = 3CF hex; index = 00 hex

<u>Bit</u>	<u>Description</u>
0-3	This field represents the value written to all 8 bits of the respective memory map when the system CPU does a memory write with write mode 0 selected and Set/Reset mode is enabled for the corresponding map. However, in write mode 3, enable Set/Reset register has no effect.
4-7	Reserved

ENABLE SET/RESET REGISTER

Port address = 3CF hex; index = 01 hex

<u>Bit</u>	<u>Description</u>
0-3	Enable Set/Reset - This field enables the set/reset function. 0 = If write mode is 0 and Set/Reset is not enabled on a map, that map is written with the value of the system CPU. 1 = If write mode is 0 and Set/Reset is enabled on a map, The respective memory is written with the value of the Set/Reset register.
4-7	Reserved

COLOR COMPARE REGISTER

Port address = 3CF hex; index = 02 hex

<u>Bit</u>	<u>Description</u>
0-3	This field represents a 4-bit color value to be compared. If the system CPU sets read mode 1 in the graphics section and does a memory read, the data returned from the memory cycle will be a 1 in each bit position where the 4 maps equal the Color compare register. All the bits of the corresponding map's byte are compared with the value of the color compare bit. Each of the 8-bit positions of the selected byte are then compared across the 4 maps and a 1 is returned in each bit position where the bits of all 4 maps equal their respective color compare values.
4-7	Reserved

DATA ROTATE REGISTER

Port address = 3CF hex, index = 03 hex

<u>Bit</u>	<u>Description</u>
0-2	This field represents a binary encoded value of the number of positions to right-rotate the system CPU data bus during system CPU memory writes. This position occurs before any other logical operation on the data takes place. This operation is done when write mode is 0. To write non-rotated data the system CPU must select a count of 0.
3,4	Function Select - Data written to memory can operate logically with data already in the system CPU latches. The bit functions are defined as follows:
<u>Bit4</u>	<u>Bit3</u> <u>Function</u>
0	0 Data unmodified
0	1 Data ANDed with latch data
1	0 Data ORed with latch data
1	1 Data XORed with latch data
5-7	Reserved

READ MAP SELECT REGISTER

Port address = 3CF hex; index = 04 hex

<u>Bit</u>	<u>Description</u>
------------	--------------------

- 0,1 Map Select - This field represents a binary encoded value of the memory map number from which the system CPU reads data. This register has no effect on the color compare read mode. In odd/even modes the value may be 00 or 01 (10 or 11) for chained maps 0,1 (2,3).
- 2-7 Reserved

GRAPHICS MODE REGISTER

Port address = 3CF hex; index = 05 hex

Bit Description
 0,1 Write Mode - The function specified by the Function Select register is applied to data being written to memory following modes 0,2 and 3 below. The bit functions are defined as follows:

<u>Bit1</u>	<u>Bit0</u>	<u>Description</u>
0	0	Each memory map is written with the system CPU data rotated by the number of counts in the Rotated register, unless Set/Reset is enabled for the map. Maps for which Set/Rest is enabled are written with 8-bits of the value contained in the Set/Reset register for that map.
0	1	Each memory map is written with the contents of the system CPU latches. These latches are loaded by a system CPU Read operation.
1	0	Memory map n (0-3) is filled with 8-bits of the value of data bit n.
1	1	Each map is written with 8-bits of the value contained in the Set/Reset register for that map (Enable Set/Reset register has no effect). Rotated system CPU data is ANDed with the Bit Mask register data to form an 8-bit value that performs the same function as the Bit Mask register does in write modes 0 and 2.
2		Reserved
3		Read Type
0 =		The system microprocessor reads data from the memory map selected by the Read Map Select register. Read Map Select register has no effect if

- bit 4 of the Sequencer Memory Mode register equals 1.
- 1 = The system microprocessor reads the results of the comparison of the 4 memory maps and the Color Compare register.
- 4 Odd/Even
- 0 = Normal VGA mode.
- 1 = Selects the odd/even addressing mode used to emulate the IBM CGA compatible modes.
- 5 Shift Register - A logical 1 instruct the Shift registers in the graphics section to format the serial data stream with even-numbered bits from both maps on the even-numbered maps and odd-numbered bits from maps on the odd maps. This bit used for modes 4 and 5.
- 6 256 Color Mode
- 0 = Allows bit 5 to control the loading of the Shift registers.
- 1 = Causes the Shift register to be loaded in a manner that supports the 256-color mode.
- 7 Reserved

MISCELLANEOUS REGISTER

Port address = 3CF hex; index = 06 hex

<u>Bit</u>	<u>Description</u>						
0	Graphics Mode - This bit controls text mode addressing control. 0 = Selects text mode operation. 1 = Selects graphics mode. When this mode is selected, the character generator address latches are disabled.						
1	Odd/Even 0 = Standard VGA addressing. 1 = Replacement system CPU address bit 0 with a higher-order address bit and select odd/even maps with odd/even values of the system CPU A0 bit, respectively.						
2,3	Memory Map - This field controls the mapping of the regenerative buffer into the system CPU address space. The bits are defined as follows: <table border="1"> <thead> <tr> <th><u>Bit3</u></th> <th><u>Bit2</u></th> <th><u>Function</u></th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>Hex A0000 for 128K bytes</td> </tr> </tbody> </table>	<u>Bit3</u>	<u>Bit2</u>	<u>Function</u>	0	0	Hex A0000 for 128K bytes
<u>Bit3</u>	<u>Bit2</u>	<u>Function</u>					
0	0	Hex A0000 for 128K bytes					

0	1	Hex A0000 for 64K bytes
1	0	Hex B0000 for 32K bytes
1	1	Hex B8000 for 32K bytes

4-7 Reserved

COLOR DON'T CARE REGISTER

Port address = 3CF hex; index = 07 hex

<u>Bit</u>	<u>Description</u>
0	Map 0 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.
1	Map 1 0 = Don't participate in the color compare cycle. 1 = Participate in the color compare cycle.

ATTRIBUTE CONTROLLER REGISTER

ATTRIBUTE ADDRESS REGISTER

Port address = 3C0 hex

<u>Bit</u>	<u>Description</u>
0-4	Attribute Address Bits - These bits point the other registers in the Attribute section. The address and data registers share the same I/O address during write operation. An international address flip-flop controls this selection. To initialize the flip-flop, an I/O Read instruction must be sent to the Attribute Controller at address 03BA or 03DA. This clears the flip-flop, and selects the Address register. After the Address register has been loaded with a write operation to 03CO, the next I/O write 03CO loads the Data register. The flip-flop toggles each time an I/O write instruction is sent to the Attribute controller.
5	Palette Address Source - Bit 5 must be cleared to 0 when loading the color Palette register. For normal operation, bit 5 is set to 1. This enables the video memory data to access the palette registers.
6,7	Reserved

PALETTE REGISTERS HEX 00 THROUGH OF

Port address = 3C1 hex; Write address = 3C0 hex; index 00-0f hex

<u>Bit</u>	<u>Description</u>
0-5	Palette - These Bits allow a dynamic mapping between the text attribute or graphic color input value and the display color on the CRT screen. A logical 1 selects the appropriate color. The palette registers should be modified only during the vertical retrace interval to avoid problems with the display image. These internal Palette register values are sent off the chip to the video DAC, where they in turn serve as addresses into the DAC internal registers.
6,7	Reserved

ATTRIBUTE MODE CONTROL REGISTER

Port address = 3C1 hex; Write address = 3C0 hex; index
10 hex

<u>Bit</u>	<u>Description</u>
0	Graphics/Alphanumeric Mode 0 = Selects alphanumeric mode. 1 = Selects graphics mode.
1	Mono Emulation 0 = Color emulation mode is set. 1 = Monochrome mode is set.
2	Enable line Graphics Character Codes 0 = The ninth dot will be the same as the background. 1 = Enables the special line graphics character codes for Monochrome emulation mode. When enabled, this bit forces the ninth dot of a line graphic character to be identical to the eighth dot of the character, line graphics character modes for the Monochrome emulation mode CO hex through DF hex. For character fonts that do not use the line graphics character codes this range, bit 2 should be set to 0. Otherwise, unwanted video information will be displayed on the CRT screen.
3	Enable Blink/Select Background Intensity 0 = Selects the background intensity of the attribute input, which was available on the Monochrome and CGA adapters. 1 = Enables the blink attribute in text modes and blinking graphics modes.
4	Reserved
5	PEL Panning Compatibility 0 = Line compare has no effect on the output of the PEL register. 1 = A successful line compare in the CRT controller forces the output of the PEL Panning registers to 0 until + VSYNC occurs, at which time the output returns to its programmed value. This bit allows a selected portion of the screen to be panned.
6	PEL Width 0 = All modes except for mode 13 hex.

the

- 1 = The video pipeline is sampled so that 8-bits are available to select a color in the 256-color mode (hex 13).
- 7 P5, P4 Select - This bit selects the source for the P5 and P4 digital video bits that go off the chip.
 - 0 = P5 and P4 are the outputs of the Palette registers
 - 1 = P5 and P4 are bits 1 and 0 of the Color Select register.

OVERSCAN COLOR REGISTER

Port address = 3C1 hex; Write address = 3C0 hex; index 11 hex

<u>Bit</u>	<u>Description</u>
0-7	Overscan Color - This register determines the overscan (border) color displays on the CRT screen. This border is a band of color around the perimeter of the display area. Its width is defined by the time display enable and blank are both inactive and is not supported in the 40-column text modes or the 320-PEL graphics modes, except for the mode 13 hex.

COLOR PLANE ENABLE REGISTER

Port address = 3C1 hex; Write address = 3C0 hex; index 12 hex

<u>Bit</u>	<u>Description</u>	
0-3	Enable Color Plane - Setting any of these bits to 1 enables the respective display memory color plane.	
4,5	Video Status MUX - Selects two of the eight color outputs to be available on the status port. The combinations available and the color output wiring shown below:	
	Color Plane Register	
	<u>Bit5</u>	<u>Bit4</u>
	0	0
	0	1
	1	0
	1	1
6,7	Reserved	