

# W65C832 CPU Datasheet v2.0

Date: 9-6-10

Updated and .PDFed by [ReactiveMicro.com](http://ReactiveMicro.com) to resolve several issues with the original datasheet.

Thanks to Tom and Constantine for sharing and helping the Community!  
Without them this datasheet and all related projects that come from it would not be possible. Thanks guys!

Original location and files: [http://apple2.org.za/gswv/a2zine/Docs/CPU\\_65832](http://apple2.org.za/gswv/a2zine/Docs/CPU_65832)

The 65C832 CPU Manual in GIF Graphic format  
Copyright © 1999 by Constantine Garland

This folder contains a series of 8 bit 256 color GIF graphic files that are the copyrighted material of Constantine Garland.

TOC1.GIF through TOC5.GIF consist of the manual information, specification and data sheet signed by Woz and the table of contents. M1.GIF through M51.GIF contains the entire context of the 65C832 CPU Preliminary Manual, information, specification and diagrams and data sheets.

They may be used without any restrictions for historical information, educational, research and graphic art needs by anybody, provided no fees or money are charged for such use.

Apple IIgs Forever!  
Constantine

Subject: Re: 65832 CPU??? Apple //f???  
Date: 11 Apr 2002 04:56:36 GMT  
From: cturley2@aol.com (Cturley2)  
Newsgroups: comp.sys.apple2

Rubywand wrote asking:

<< That's a pretty rare manual. How did you obtain it?>>

;-) Legally -- by snail mail from a guy in Oklahoma that offered to send it to me for free. He told me he was a student in high school years ago and decided he wanted info on the then rumored NEW 65832 CPU for the IIGs.

He contacted WDC with his request convinced them he was a big time chip manufacture interested in buying it for commercial production and they sent him one.

I got wind of him from an offer he posted to this NG back in 1995 -- asking if anybody was interested in it for free. I emailed him first on it and he mailed it on to me promptly.

I showed it to Woz at a rock concert back in 1996 -- he was astounded when reviewing it and signed the cover page for me. That's why it has that Woz sig. on it. As such -- yes, it is pretty rare -- and -- with mine and the autograph from Woz on it's cover page --- it's a priceless and VERY rare one-of-a-kind.

WDC told me on several occasions in our many telcons: "We have no such manual our self now -- only made a dozen or so and mailed all of them out to clients many years ago." I've never found anybody else that has one either.

Mine may well be the only one left in existence now (???). That's why I digitized it \*cover to cover\* and put it online to share the info with the world.

Cheers,  
Tom

W65C832

INFORMATION, SPECIFICATION AND DATA SHEET

**PRELIMINARY**

A  
B  
O  
R  
V  
V  
R  
V  
M  
P  
M  
R  
R  
R  
R  
V  
V  
E  
V  
M  
P  
L  
Q  
T  
D  
P  
S  
S  
D  
/  
X  
I  
B  
-  
-  
-  
Y  
-  
S  
-  
A  
X  
2  
E

	6	5	4	3	2	1	44	43	42	41	40	
NMI-	7										39	E8/E16
VPA	8										38	R/W-
VDD	9										37	VDD
A0	10										36	D0/A16
A1	11										35	D1/A17
VSS	12						W65C832				34	D2/A18
A2	13										33	D3/A19
A3	14										32	D4/A20
A4	15										31	D5/A21
A5	16										30	D6/A22
A6	17										29	D7/A23
	18	19	20	21	22	23	24	25	26	27	28	
	A	A	A	A	A	V	V	A	A	A	A	
	7	8	9	1	1	S	S	1	1	1	1	
				0	1	S	S	2	3	4	5	

*Woz*

## TABLE OF CONTENTS

<hr/>	
<b>INTRODUCTION</b>	<b>1</b>
<hr/>	
<b>SECTION 1: W65C832 FUNCTION DESCRIPTION</b>	<b>2</b>
1.1 Instruction Register and Decode . . . . .	2
1.2 Timing Control Unit . . . . .	2
1.3 Arithmetic and Logic Unit . . . . .	2
1.4 Internal Registers. . . . .	2
1.5 Accumulators. . . . .	3
1.6 Data Bank Register. . . . .	3
1.7 Direct. . . . .	3
1.8 Index . . . . .	3
1.9 Processor Status. . . . .	3
1.10 Program Bank Register . . . . .	4
1.11 Program Counter . . . . .	4
1.12 Stack Pointer . . . . .	4
<hr/>	
<b>SECTION 2: PIN FUNCTION DESCRIPTION</b>	<b>10</b>
2.1 Abort . . . . .	.11
2.2 Address Bus . . . . .	.11
2.3 Bus Enable. . . . .	.11
2.4 Data/Address Bus. . . . .	.11
2.5 Emulation Status. . . . .	.12
2.6 Interrupt Request . . . . .	.12
2.7 Memory Lock . . . . .	.12
2.8 Memory/Index Select Status. . . . .	.12
2.9 Non-Maskable Interrupt. . . . .	.12
2.10 Phase 2 In. . . . .	.12
2.11 Read/Write. . . . .	.13
2.12 Ready . . . . .	.13
2.13 Reset . . . . .	.13
2.14 Valid Data Address, Valid Program Address . . . . .	.14
2.15 VDD and VSS . . . . .	.14
2.16 Vector Pull . . . . .	.14
<hr/>	
<b>SECTION 3: ADDRESSING MODES</b>	<b>15</b>
3.1 Reset and Interrupt Vectors . . . . .	.15
3.2 Stack . . . . .	.15
3.3 Direct. . . . .	.15
3.4 Program Address Space . . . . .	.15
3.5 Data Address Space. . . . .	.15































































































































